2022年1月13日＠SPring-8次世代先端研究会
SPring-8先端利用技術ワークショップ

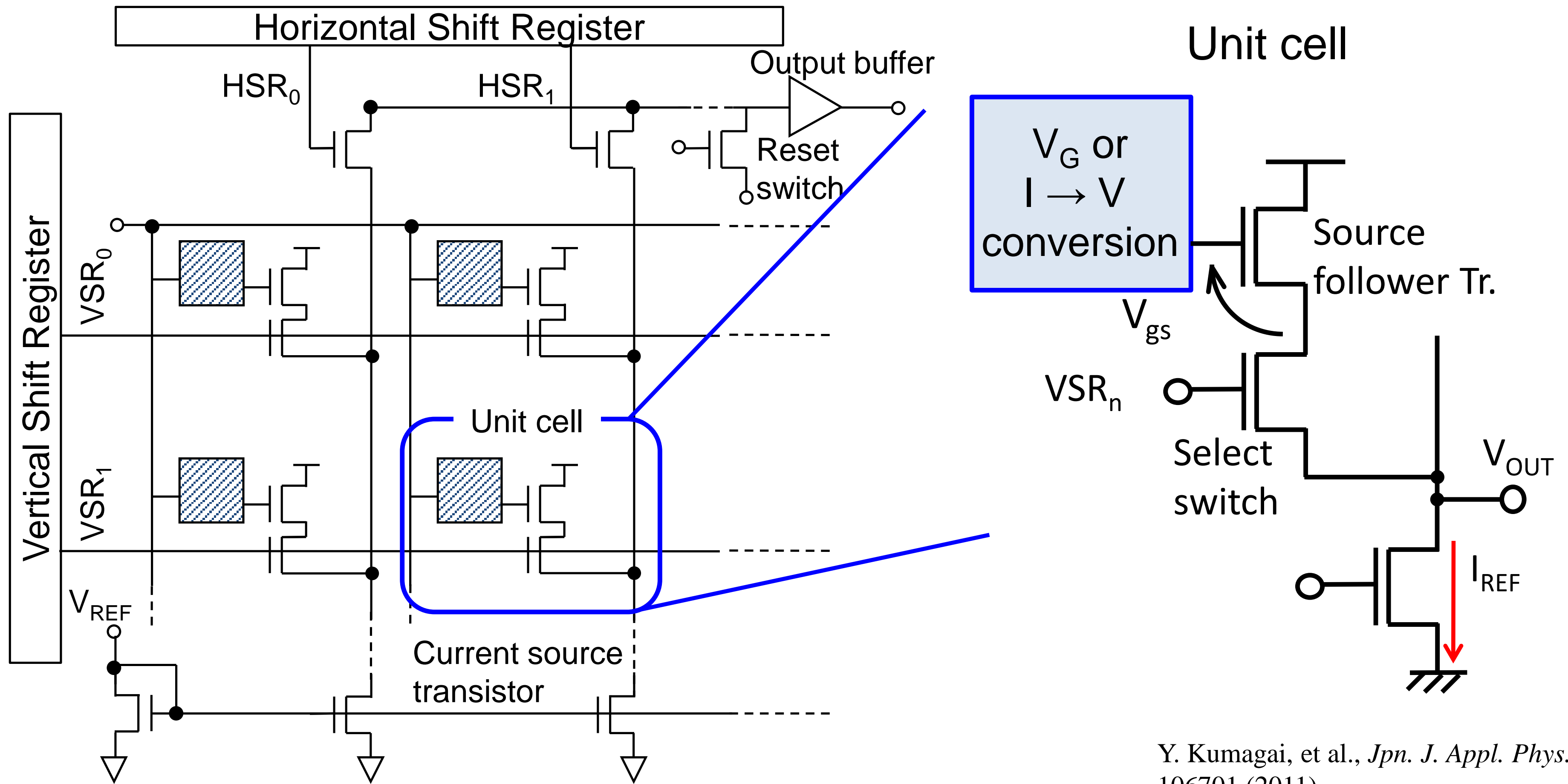
広島大学

集積回路における半導体トランジスタのバラツキ・雑音について

広島大学ナノデバイス・バイオ融合科学研究所
所長・教授　寺本 章伸

Measurement method

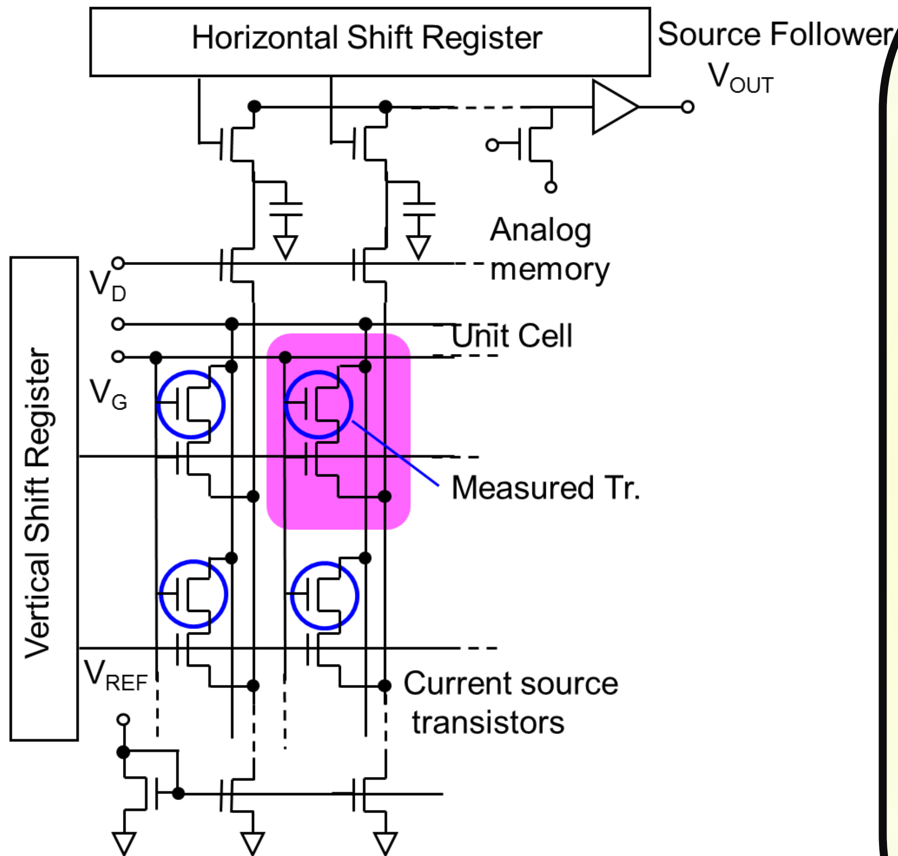
基本的なテスト回路



Y. Kumagai, et al., *Jpn. J. Appl. Phys.*, 50, 106701 (2011)

ソースフォロア回路によって回路内で電流を電圧信号に変換
電圧信号は増幅された後、外部に出力

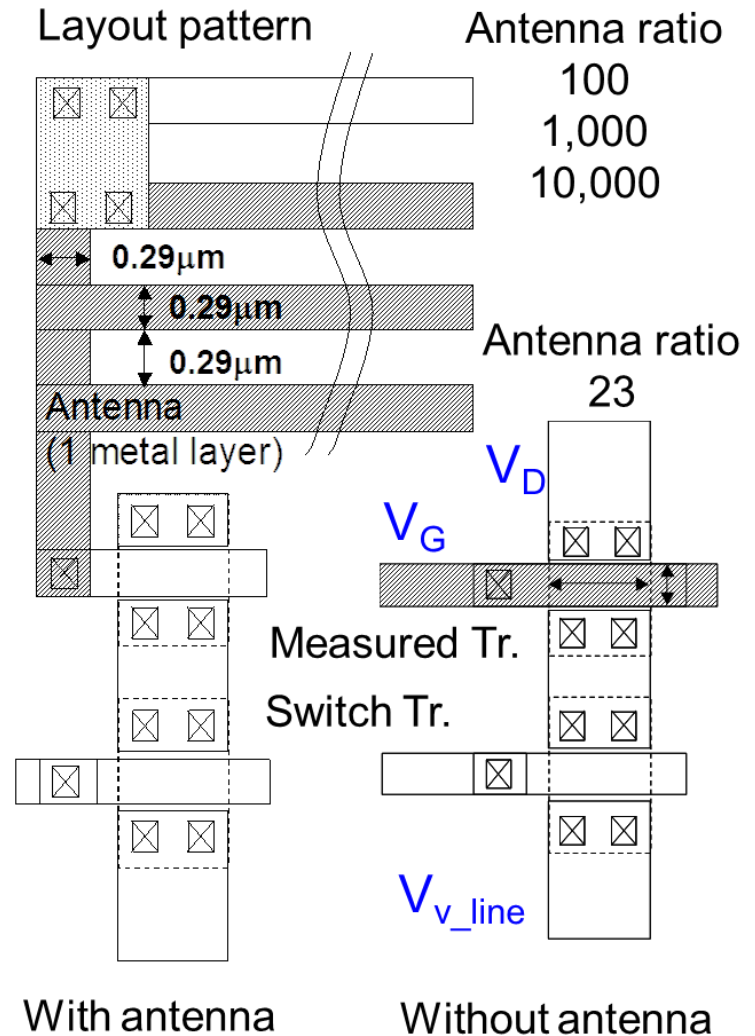
Circuit schematic view of test structure



- Arrayed measured Tr. and select switch Tr.
  ⇒easy to integrate many Trs.
- Simple peripheral circuit
  ⇒operating in a wide range to measure various Trs. with L, W, gate insulator, its thickness,…
- Read-out and charging vertical line in parallel
  ⇒rapid measurement

Test Structure

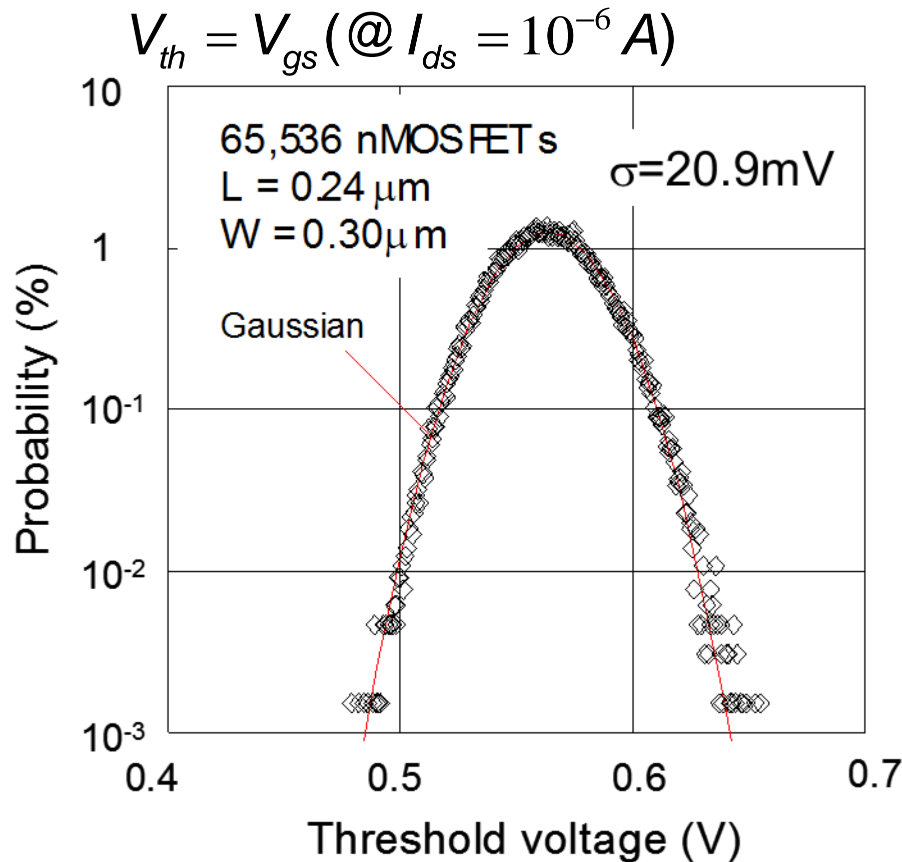
Process	0.22μm 1-poly 2-metal standard CMOS process
Number of Tr.	1,258,816 (nMOS) 786,760 (pMOS)
Number/ 1 size	131,072 81,920
Type of Tr.	21
	nMOS, pMOS
Unit cell area	5μm × 5μm (nMOS) 7.5μm × 5μm (pMOS)
Reading time	0.7sec/shot
TEG size	5.5 × 14 mm^2
Pad number	16

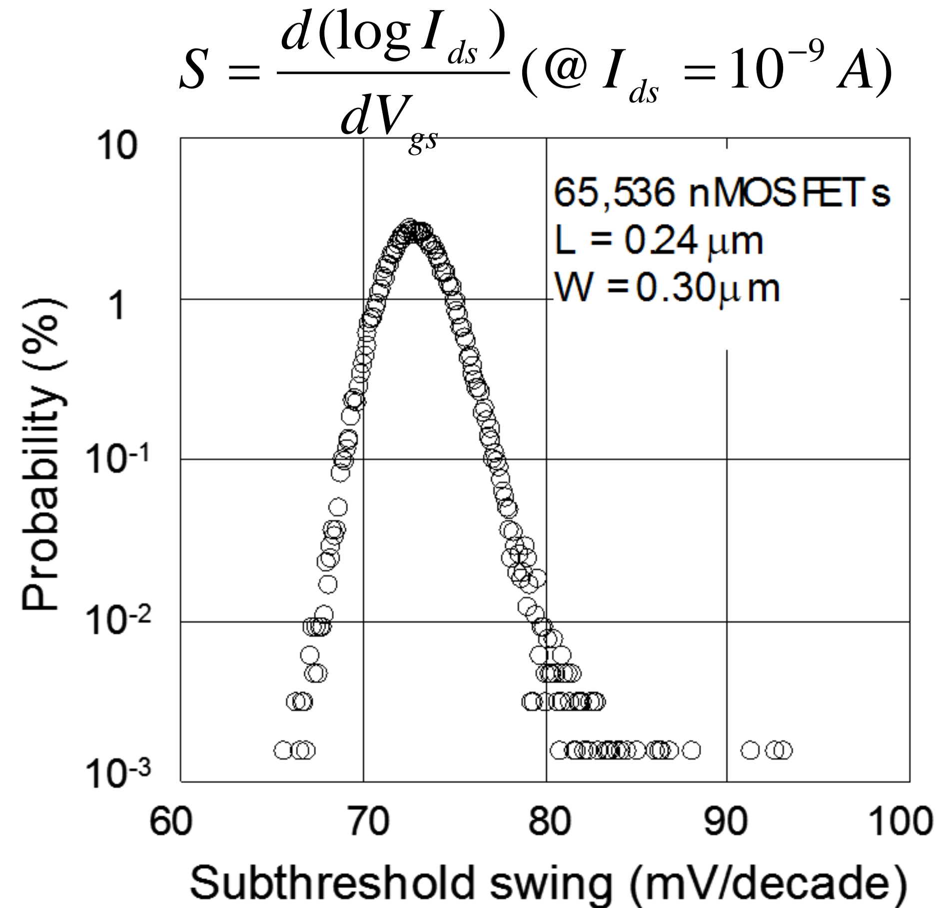


It is possible to measure various type MOSFETs

MOSFETの特性バラツキ

Distribution of threshold voltages and S-factors

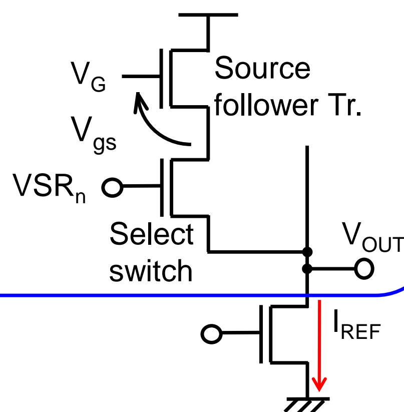




We can evaluate distribution of V_{th} and S-factor easily.

Wafer Map of Vth

Unit cell



Gate length L (mm)	Gate width W(mm)	Number of transistors
0.22	0.28	65,536 (64x1024)
0.22	0.30	65,536 (64x1024)
0.24	0.30	65,536 (64x1024)
0.24	1.5	65,536 (64x1024)
0.24	15	16,384 (64x256)
0.40	15	16,384 (64x256)
0.40	1.5	65,536 (64x1024)
1.2	0.30	32,768 (32x1024)
1.2	1.5	32,768 (32x1024)
4.0	0.30	32,768 (32x1024)
4.0	1.5	32,768 (32x1024)
0.24	0.30	32,768 (32x1024) Antenna ratio 100
1.2	15	8,192 (32x256)
4.0	15	8,192 (32x256)
10	15	4,096 (16x256)
0.24	0.30	4,096 (16x256) Antenna ratio 1,000
0.24	0.30	1,344 (32x42) Antenna ration 10,000

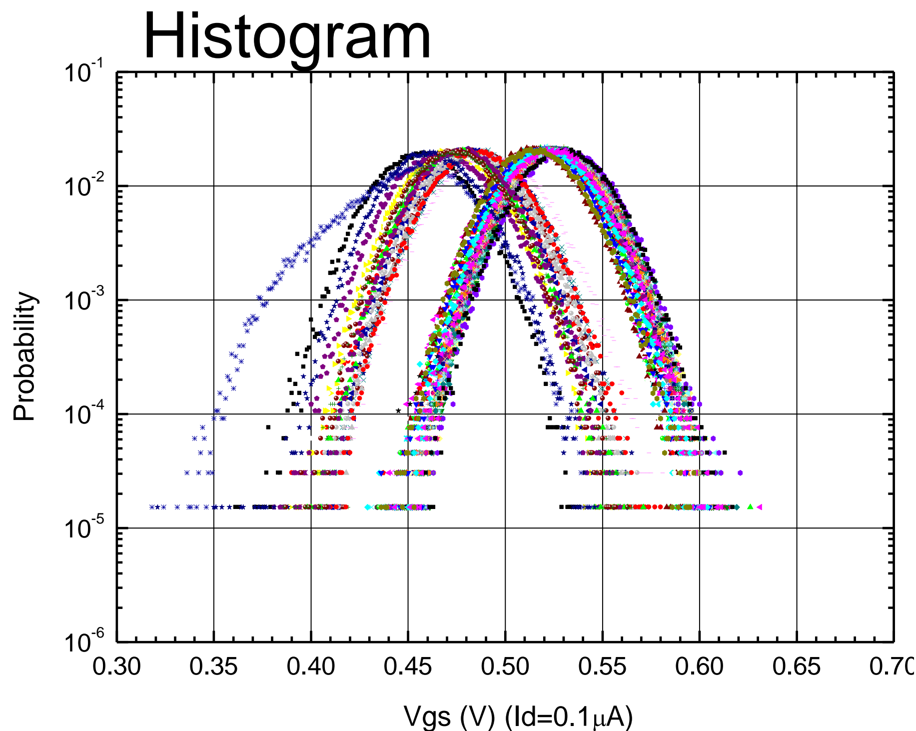
200 mm wafer

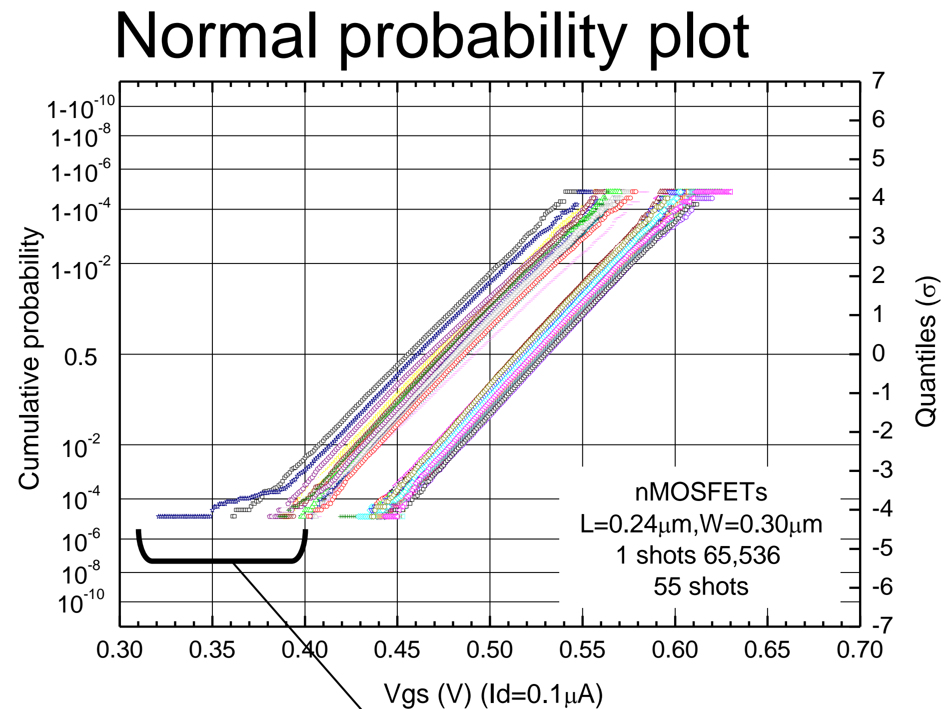
Vgs (each gate size)

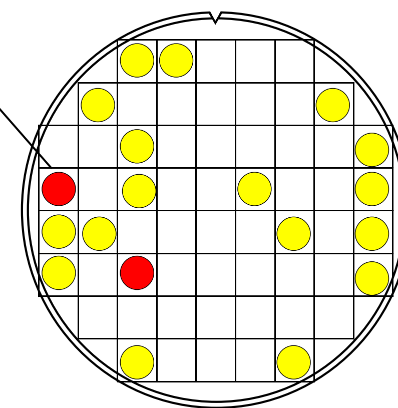
-80mV Average 80mV

S. Watabe, et al., *IEEE Trans Electron Devices,* vol. 57, p. 1310, 2010.

V_{th} Variability in a wafer





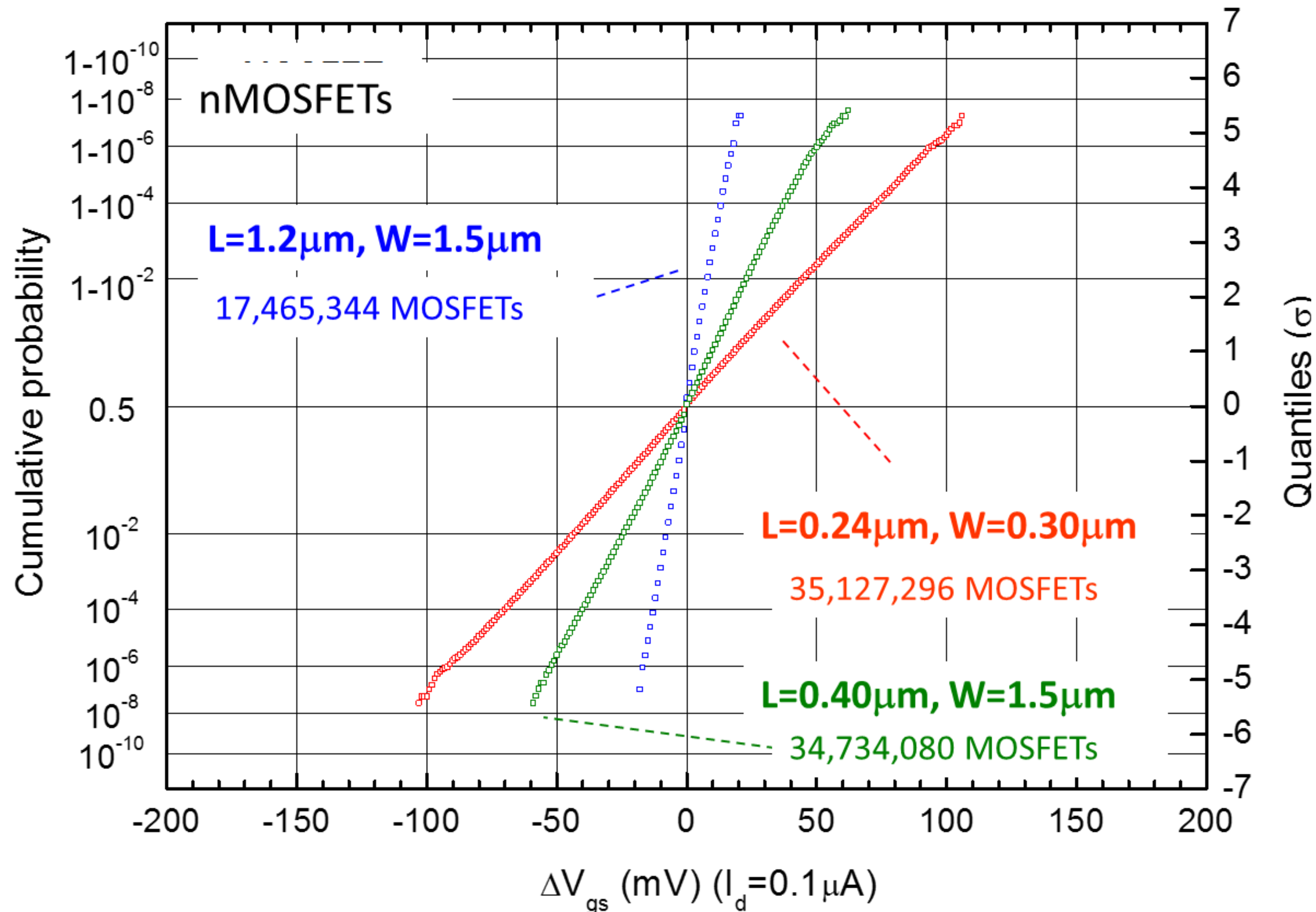


- ~300mV in a 200 mmΦ-wafer
- ~160mV in a shot
- ~80mV –Difference between the average V_{th} shot to shot

→ Variability in a shot >> shot to shot

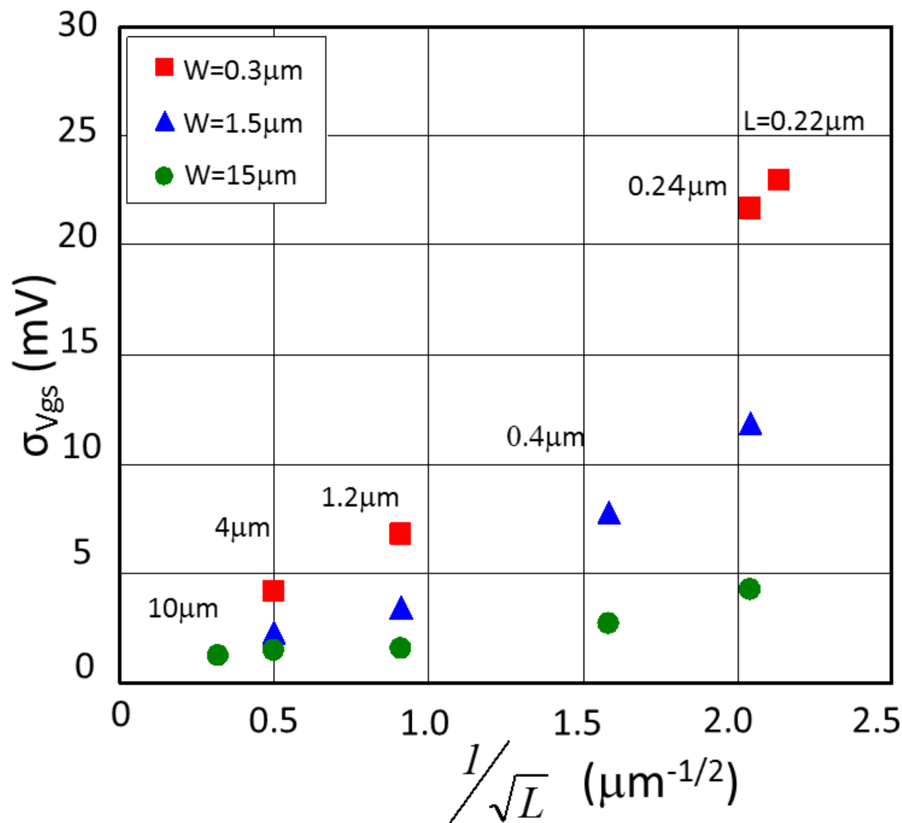
Vth Variability dependence on Gate size

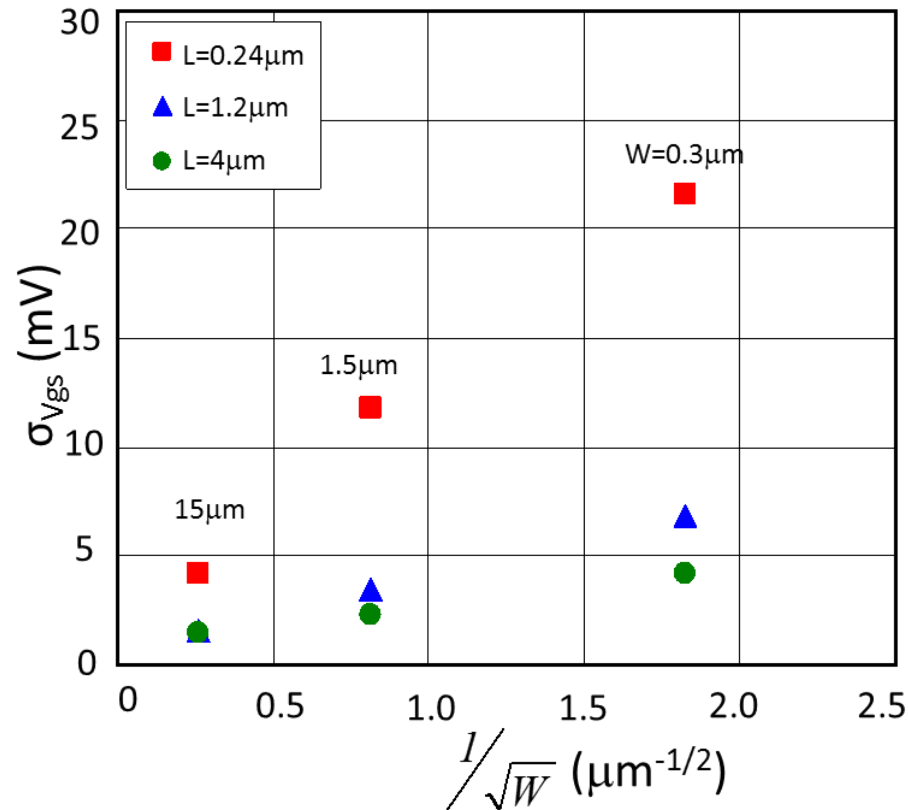
35,000,000 MOSFETs are evaluated



The V_{th} Variability follows the Normal distribution even in the tail part.
(35 Million MOSFETs, ±5.5s)

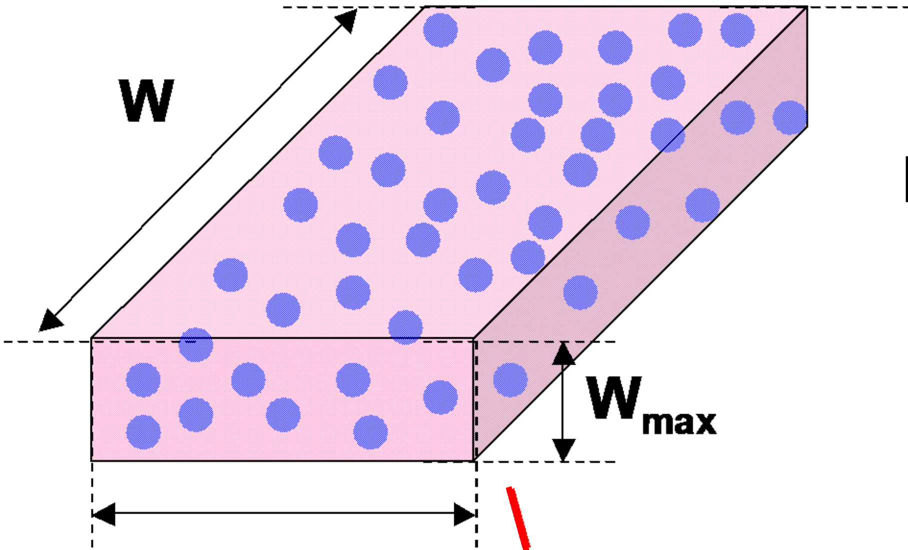
V_{th} Variability dependence on Gate size

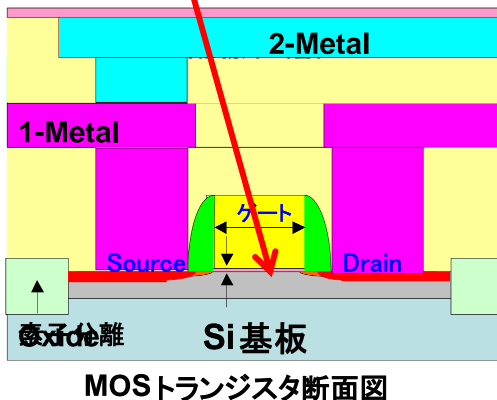




Variability increase with an increase of gate length and width.
L<0.4μm: Variability drastically increases.

Statistical Variability of impurity atom





When impurity atoms are uniformly distributed

$$L \cdot W \cdot W_{max} \cdot N_d \pm (L \cdot W \cdot W_{max} \cdot N_d)^{1/2}$$

Average　　　　　Variation : σ

Impurity concentration

1　$1.9 \times 10^{17} cm^{-3}$

2　$3.1 \times 10^{17} cm^{-3}$

3　$4.4 \times 10^{17} cm^{-3}$

Dependence of σ on impurity conc.

W/L=0.28μm/0.22μm

0.3μm/1.2μm

$\sigma(V_{gs})$ (mV)

30
25
20
15
10
5

1.0 2.0 3.0 4.0 5.0 6.0 7.0

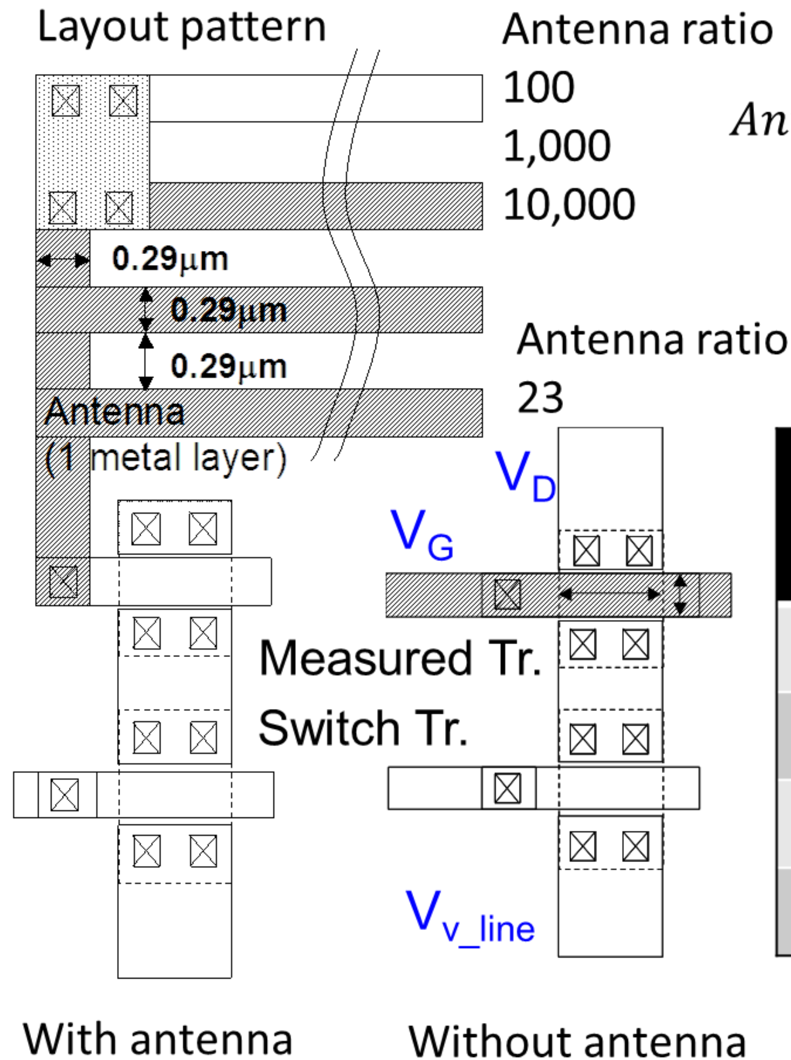
N_{sub} ($\times 10^{17}$ cm^{-3})

$$\sigma_{Vth} \approx \frac{1}{\sqrt{LW}} \left(\frac{\sqrt[4]{q^3 \varepsilon_s \phi_B N_d}}{\sqrt{2}} \right) \frac{T_{ox}}{\varepsilon_{ox}}$$

$$\sigma_{\mathrm{N_{sub}}} \propto \sqrt{\mathrm{N_{sub}}}$$

$$\mathrm{Depletionregion} \propto \frac{1}{\sqrt{\mathrm{N_{sub}}}}$$

MOSFETs Characteristics Change by Plasma Processes



Antenna ratio
100
1,000
10,000

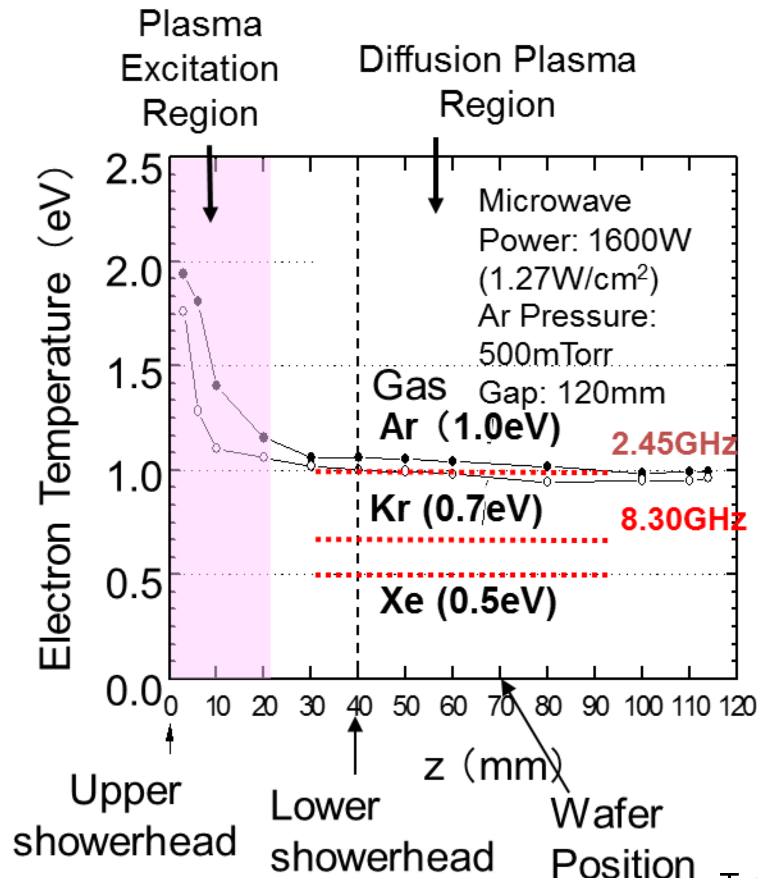
$$Antenna\ Ratio = \frac{Area\ of\ 1st\ Metal\ Laayer}{L \times W\ of\ MOSFET}$$

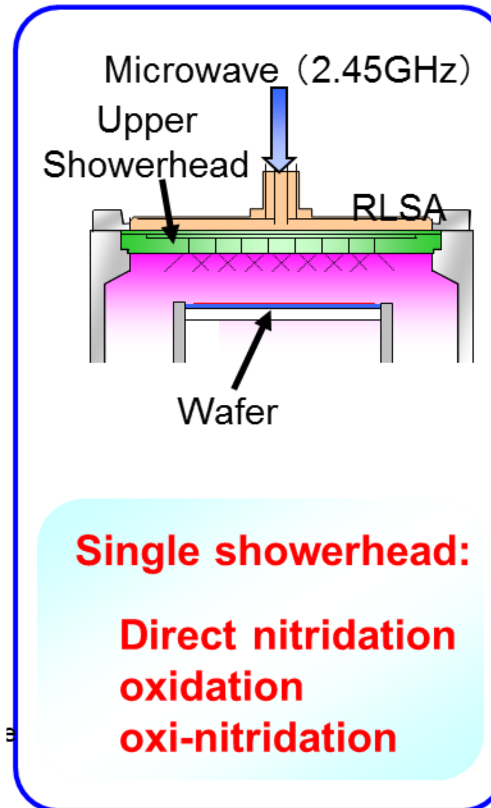
Antenna ratio
23

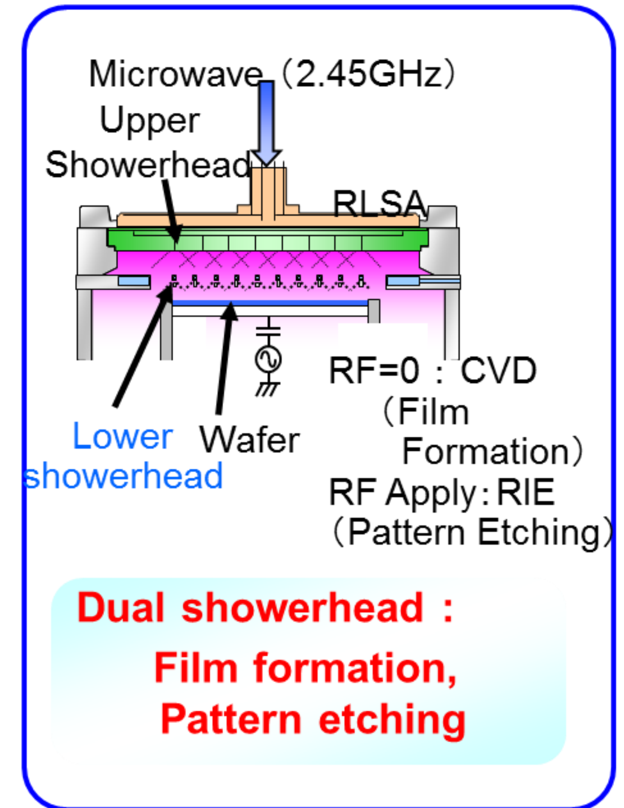
Antenna Ratio	Number of MOSFETs	
	NMOS	PMOS
23	65,536	40,960
10^2	32,768	20,480
10^3	4,096	2,560
10^4	1,344	840

Evaluation of Plasma process by antenna pattern

Microwave-Excited High-Density Plasma Equipment with the Single and the Dual-Showerhead Structure







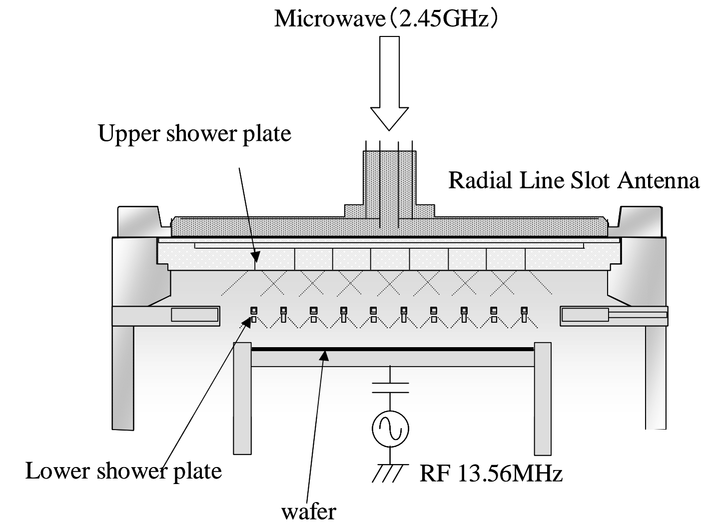
T. Ohmi, M. Hirayama, and A. Teramoto, J. Phys. D: Appl. Phys. **39** (1), R1 (2006).

- Microwave (high frequency) excited plasma → high density
- Process in diffusion plasma region → low damage

Experimental

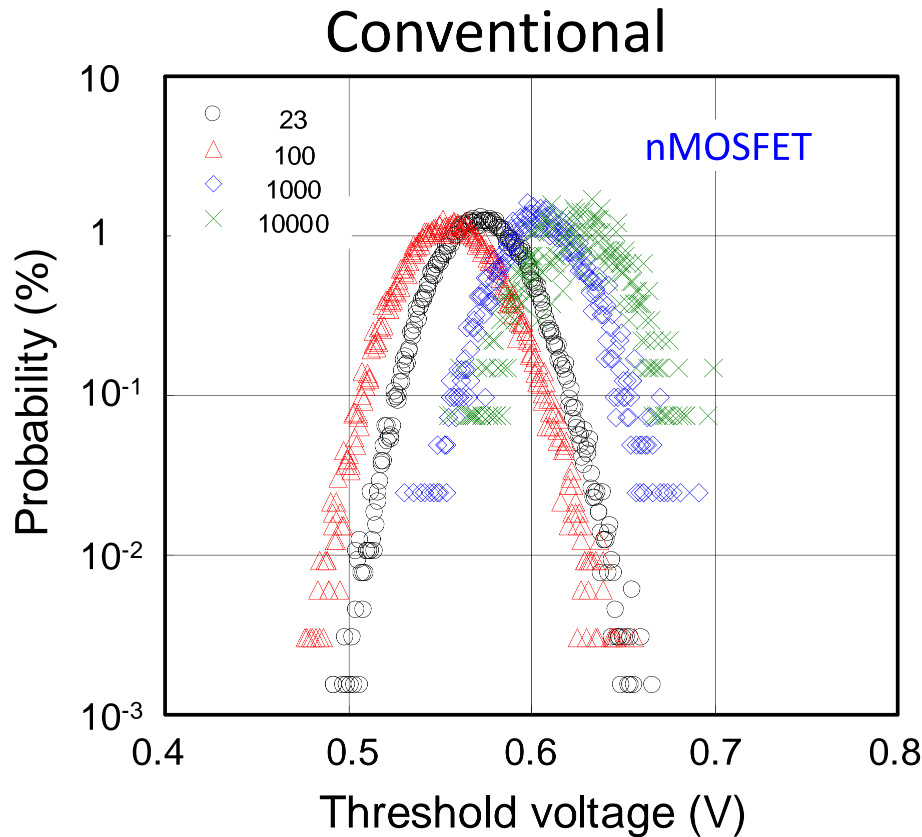
After Formation of the antenna, the damage of plasma processes were evaluated.

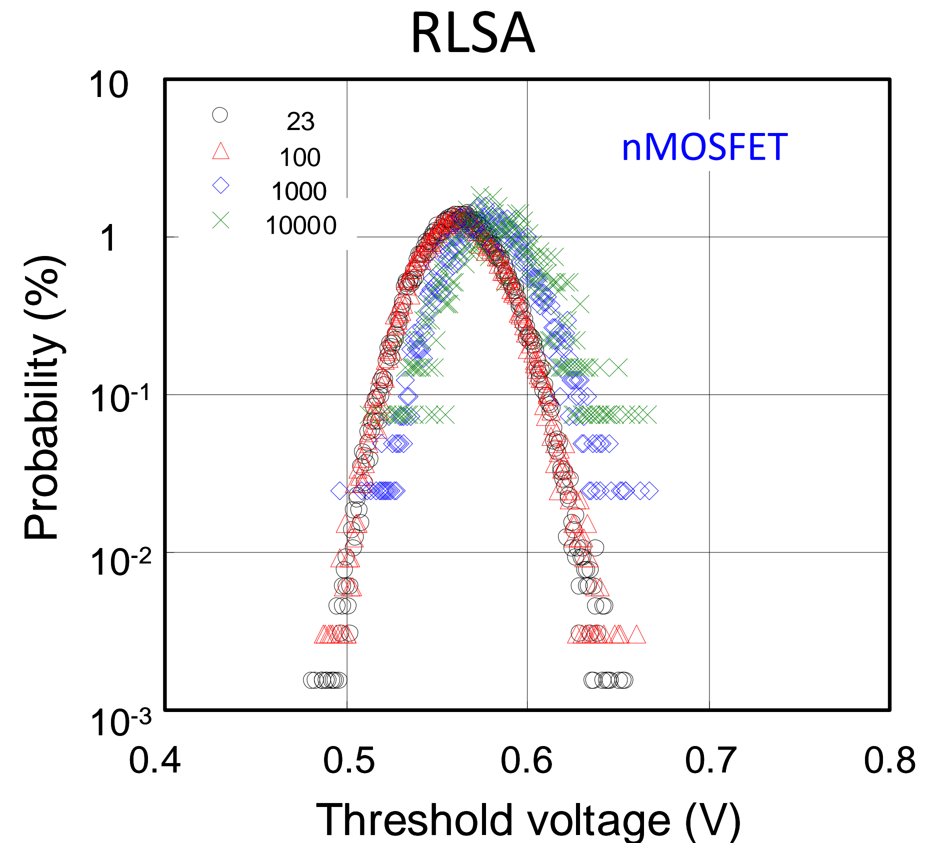
S. Watabe, et al., *IEEE Trans. Electron Devices,* 57, p. 2010.



	Conventional	RLSA
1st Metal Etching	ECR （Electron Cyclotron Resonance）	RLSA
CVD Interlayer-SiO_2 Formation M1/M2	ICP （Inductive Coupled Plasma）	RLSA
Via hole Etching interlayer of Metal1-2	Parallel Plate	RLSA

V_{th} Distribution (n-MOSFETs)

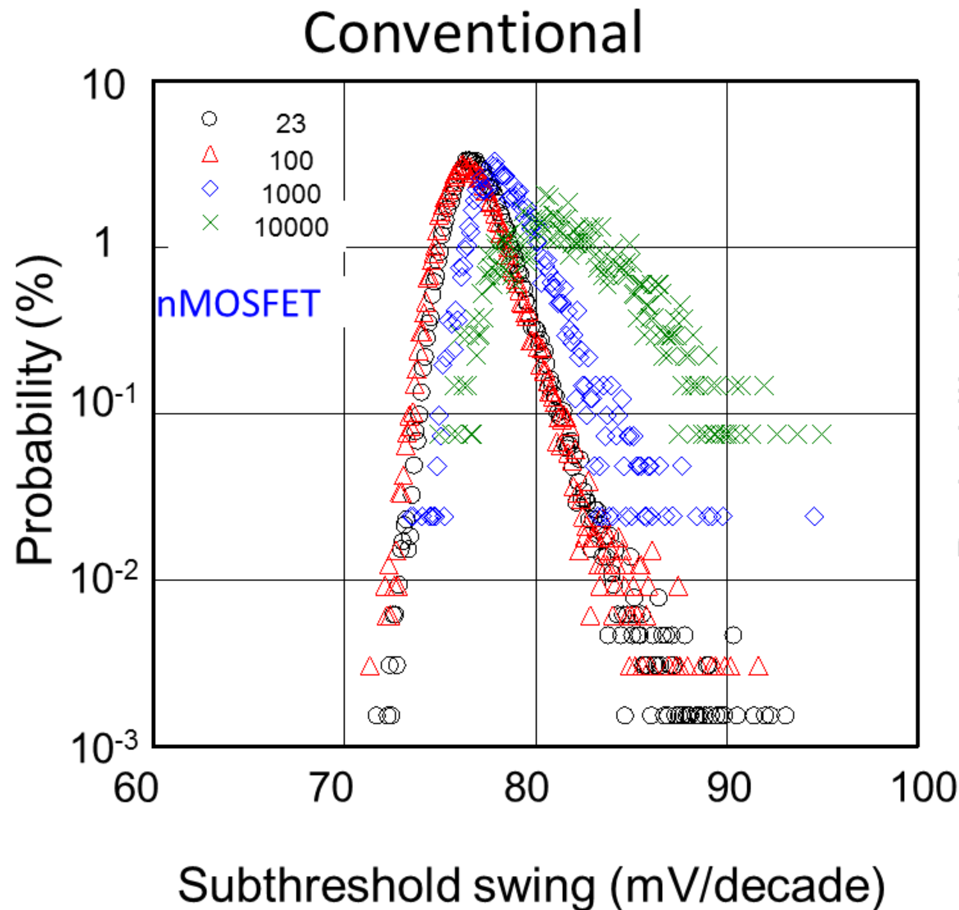


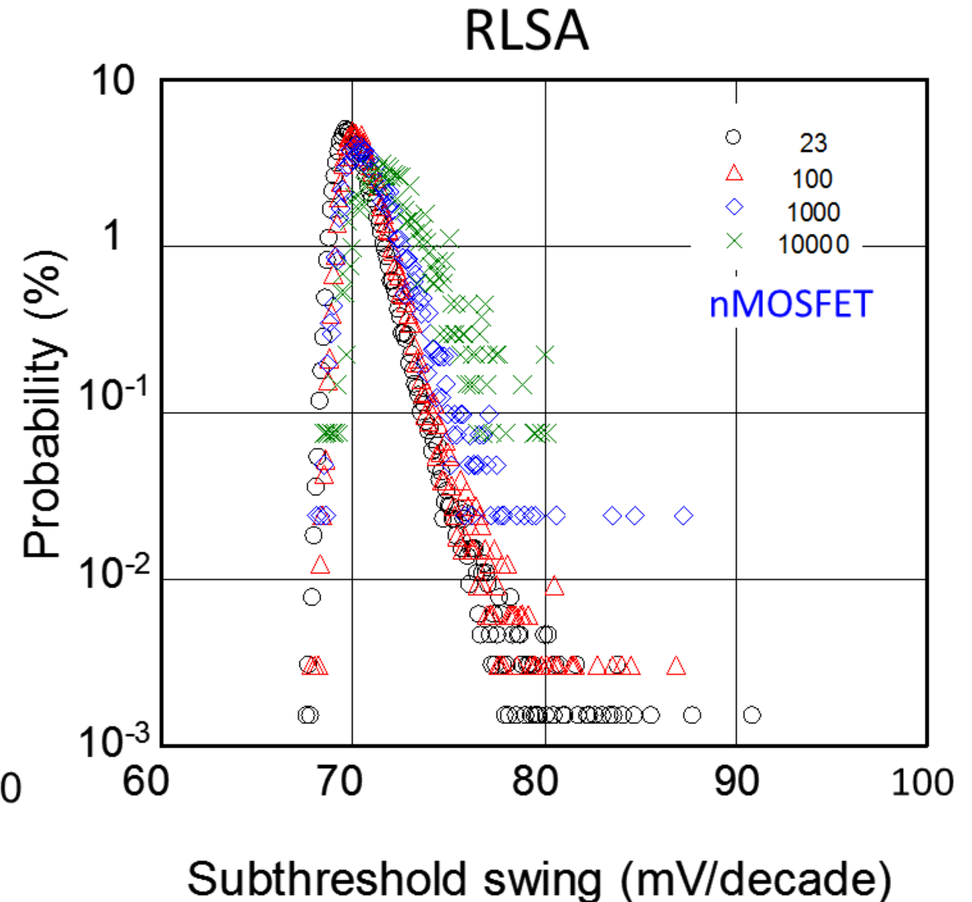


RLSA Plasma

-V_{th} shift is less than that of conventional.
- No shift less than antenna ratio less than 100.

Dependence of S-factor on antenna ratio(n-MOSFETs)



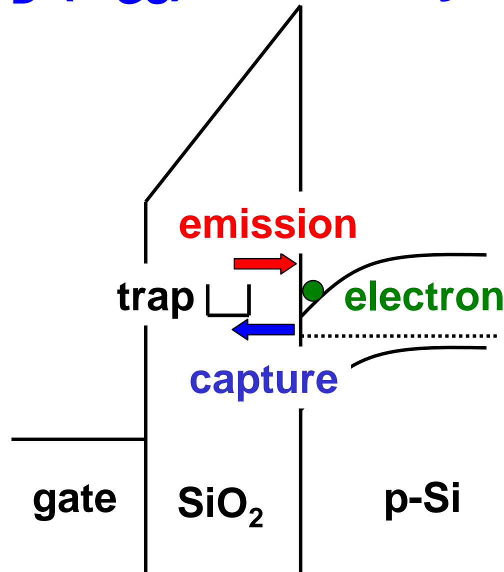


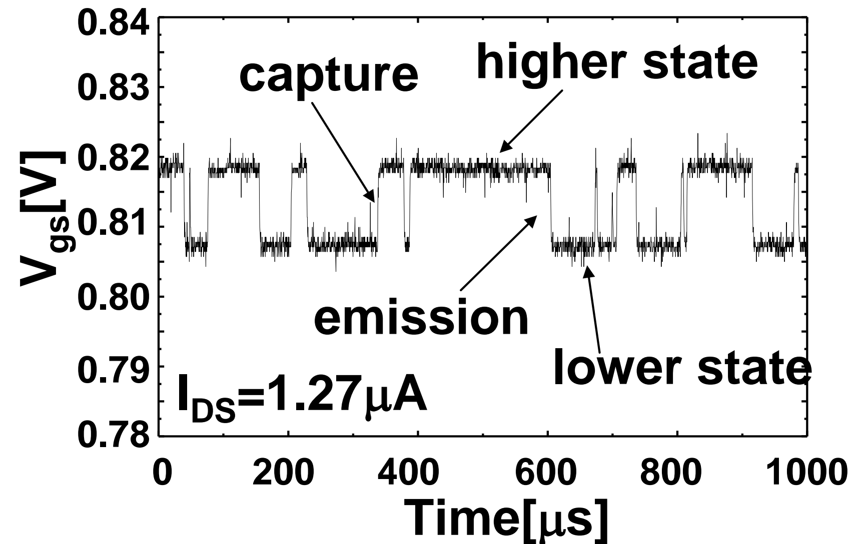
・By RLSA plasma the average value and variability are improved compared with conventional plasma.

Random Telegraph Noise (RTN)

Random Telegraph Noise (RTN)

Carrier Capture & Emission in Traps in Gate Insulator
⇒ Change of Carrier Number & Mobility
⇒ I_D (V_{GS}) randomly and discretely changes



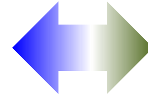


Increase of RTS by shrinkage of MOS devices causes…

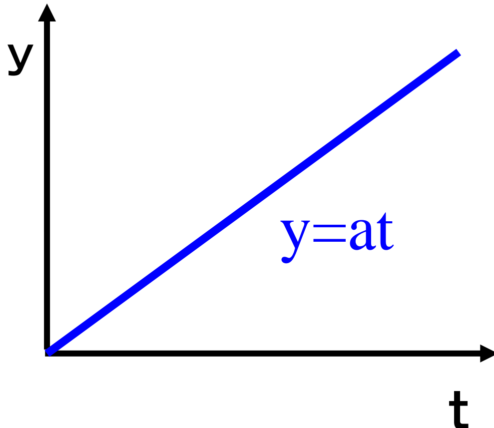
- **CMOS Image sensor***
  Signal amplitude changes in time domain ⇒Image Degradation by Twinkle noise
- **Flash memory****
  Vth variation in read time ⇒Difficult to multi-bit

アナログ信号とディジタル信号

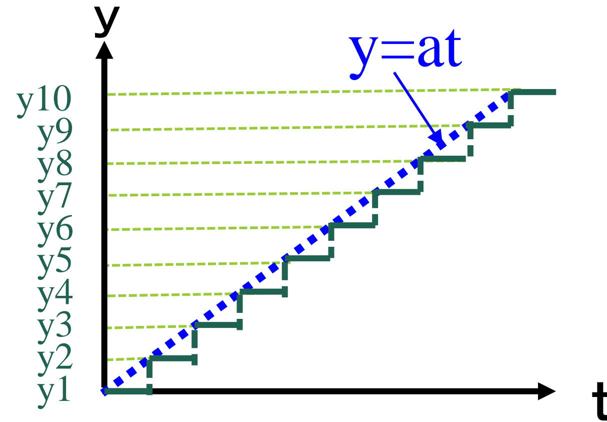
アナログ信号　:連続的に変化



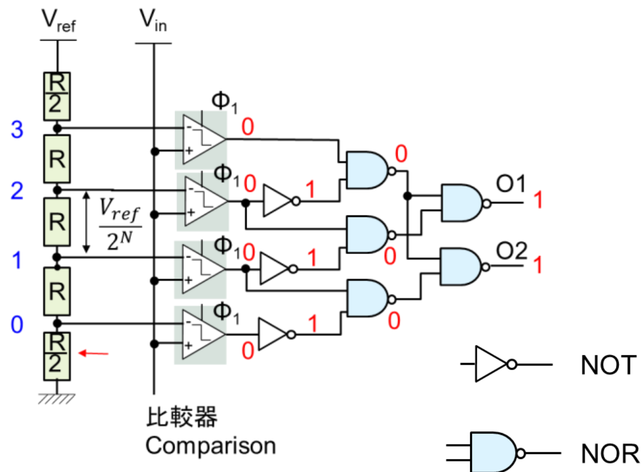
ディジタル信号　:離散的に変化



自然界



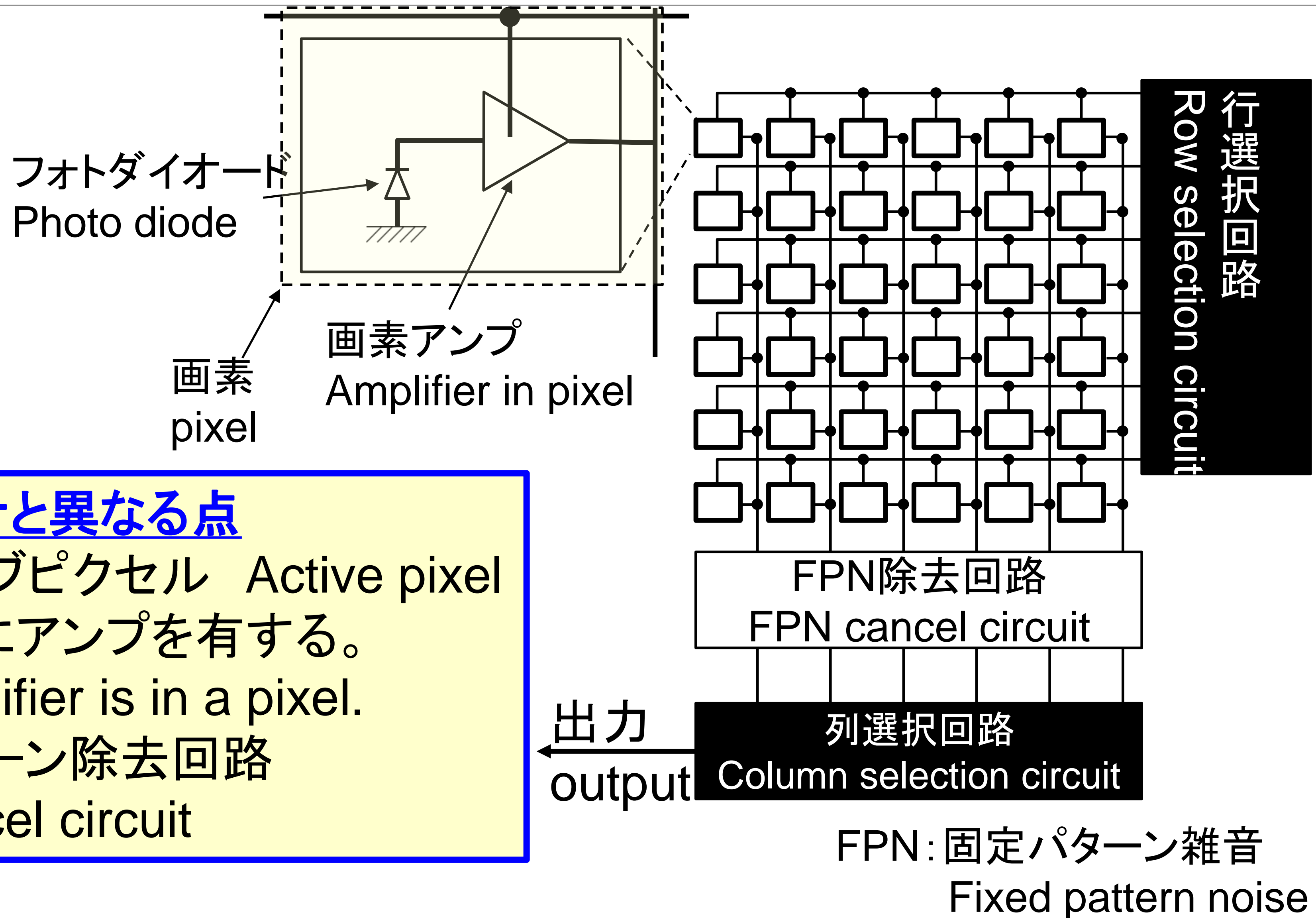
集積回路での演算



NOR

Input		Output
0	0	1
0	1	0
1	0	0
1	1	0

CMOS image sensor



MOSセンサと異なる点

- アクティブピクセル Active pixel
  画素内にアンプを有する。
  An amplifier is in a pixel.
- 固定パターン除去回路
  FPN cancel circuit

RTN Evaluation

Problems in RTS evaluation

- ◆ Appearance Probability of MOSFETs having RTS is relatively small. →Long searching time is required for unit MOSFET measurement.
- ◆ RTS characteristics show large variation for each MOSFETs. Amplitude, time constant, temperature dependence, bias dependence

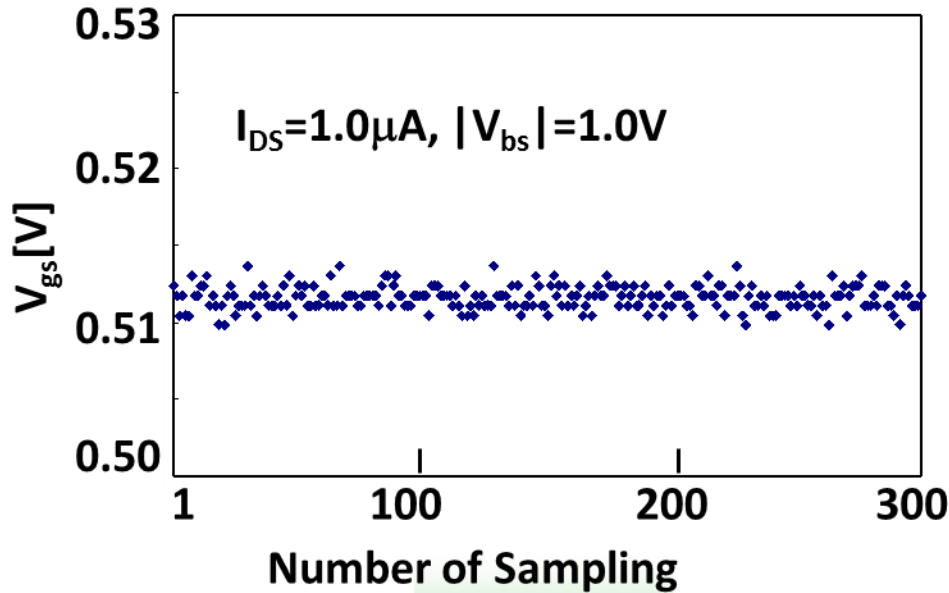
- ・Location, energy state and cross section of traps
- ・non-uniformity of channel
(Gate insulator thickness, Localization of impurity atoms)
- ・Degradation and recovery characteristics for stress

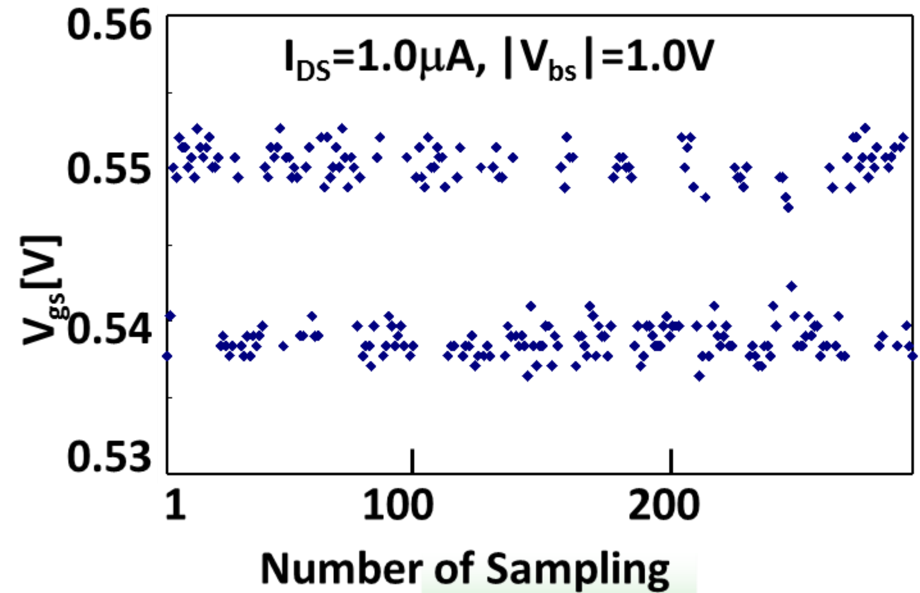
} Variation of RTS characteristics

RTS must be statistical phenomenon!!

It is essentially required that RTS is statistically evaluated.

Definition of σR – Indicator of RTN

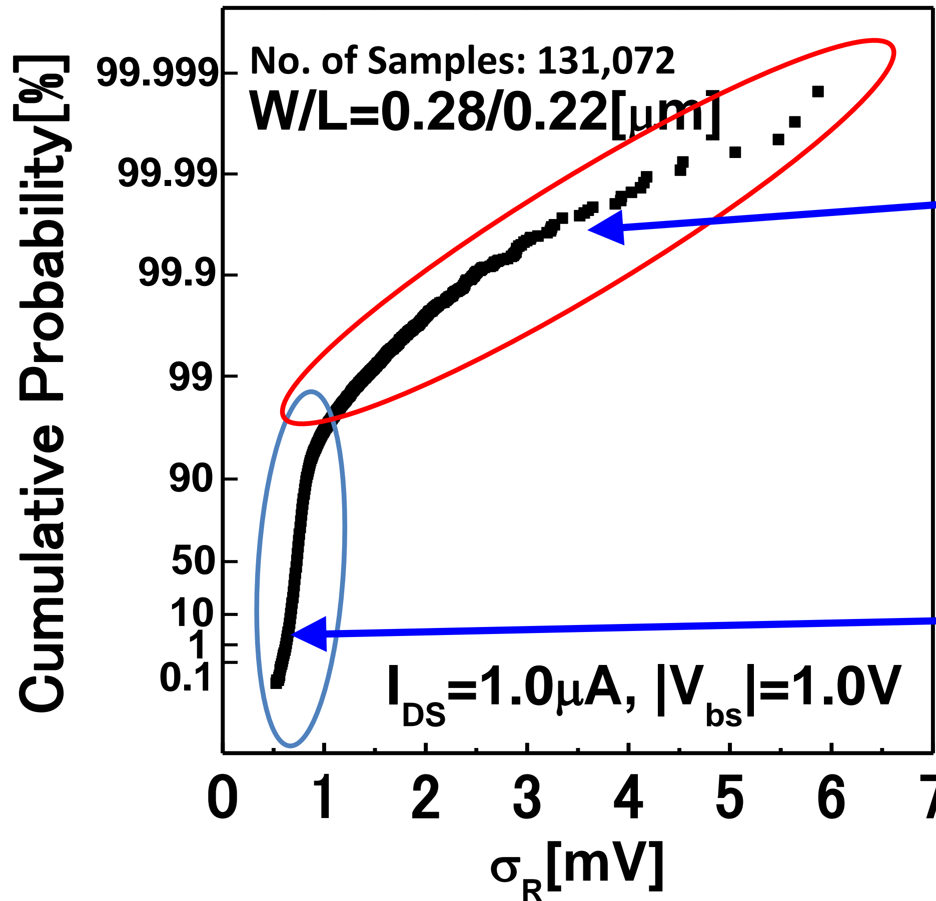


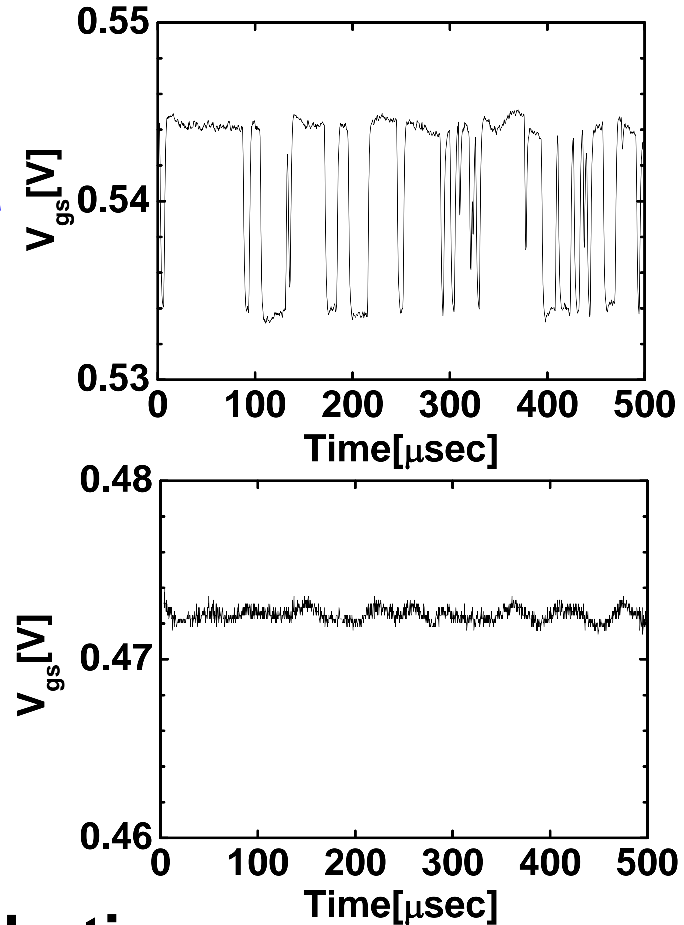


σ_R = 1.15 mV

σ_R = 9.09 mV

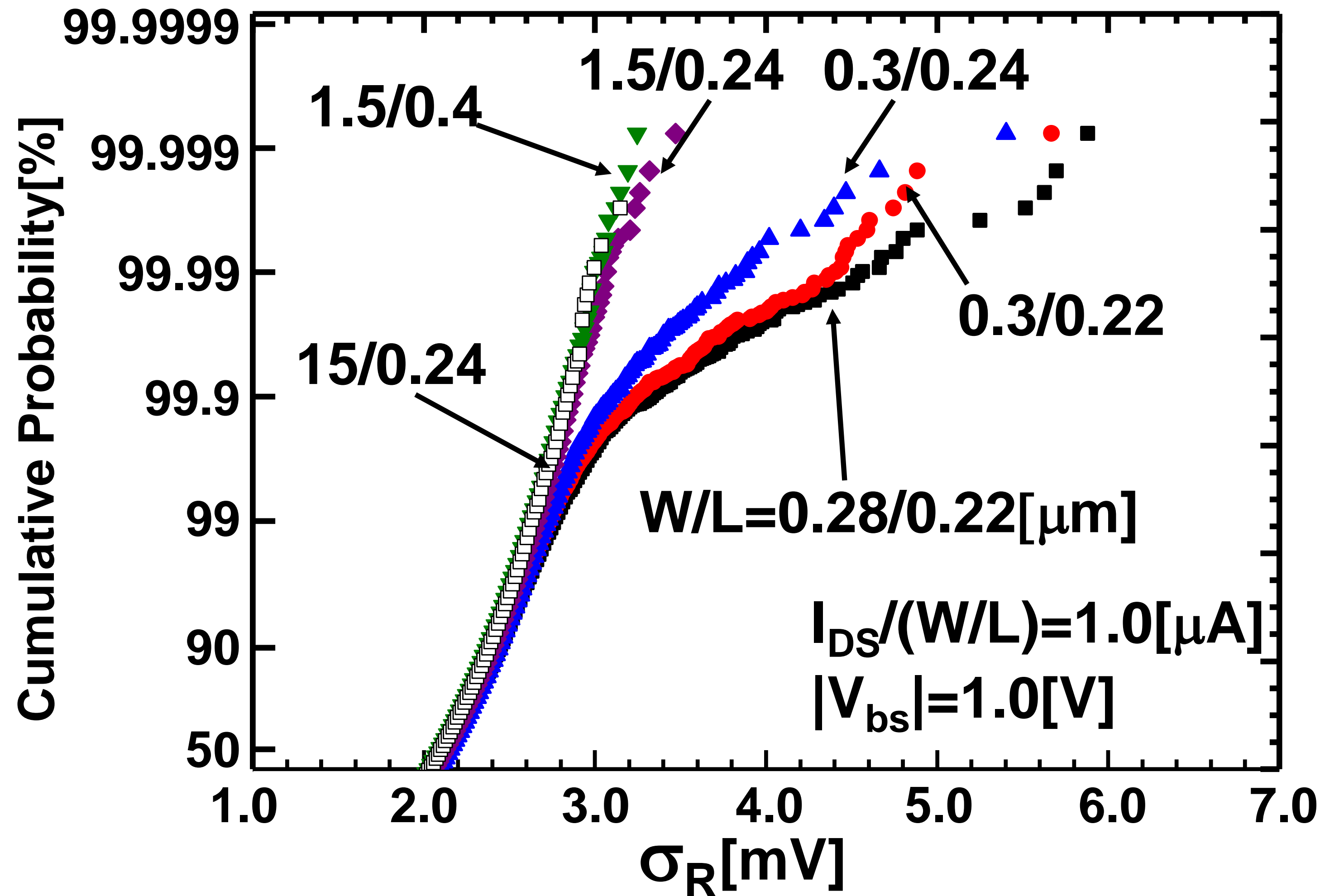
Relation between RTN waveforms and σR Distribution





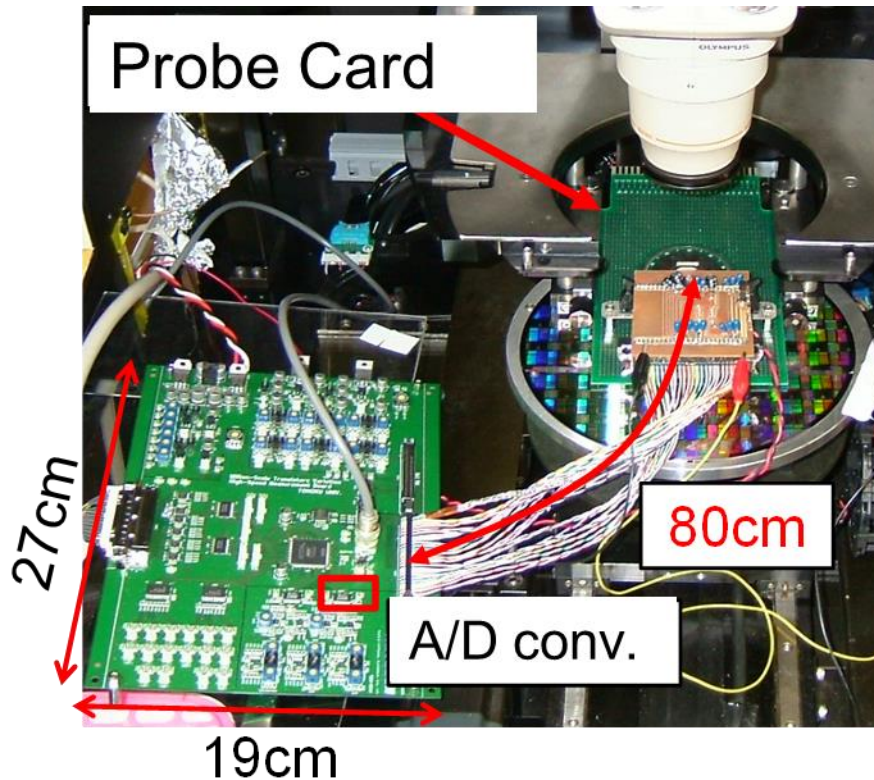
- σ_R distribution is NOT normal distribution.
- A characteristic tail spreads to the right-side. (less than 1 %)
- RTS appears in the tail part.

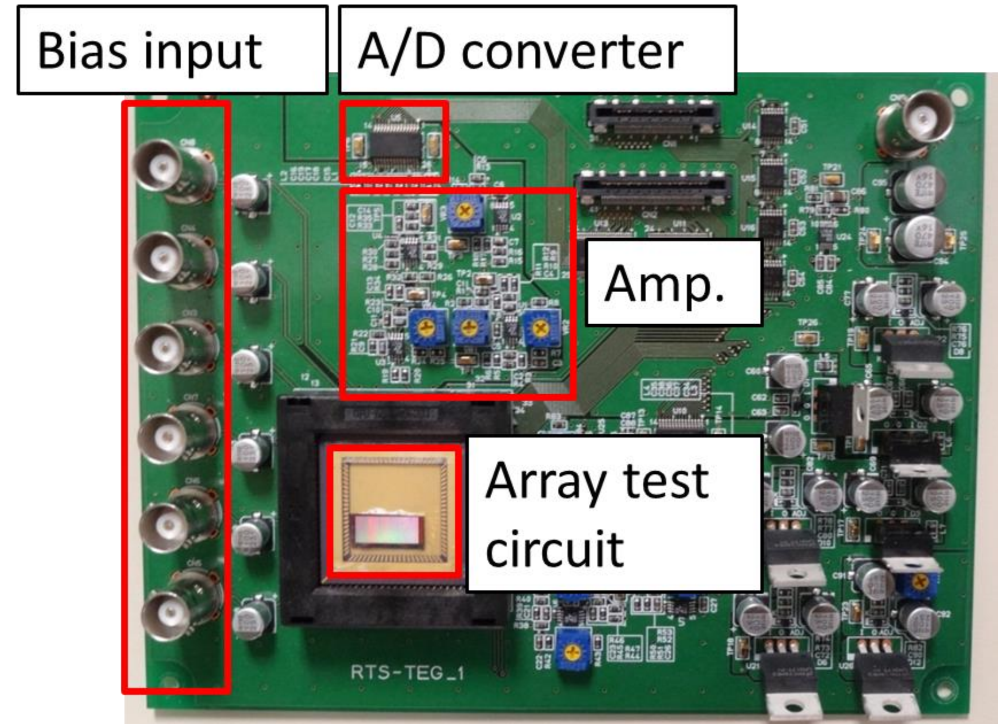
Gate Size Dependence of σR Distributions



Smaller gate size, Larger σ_R tail.
The tails follow Gumbel distribution.

Measurement system & Accuracy



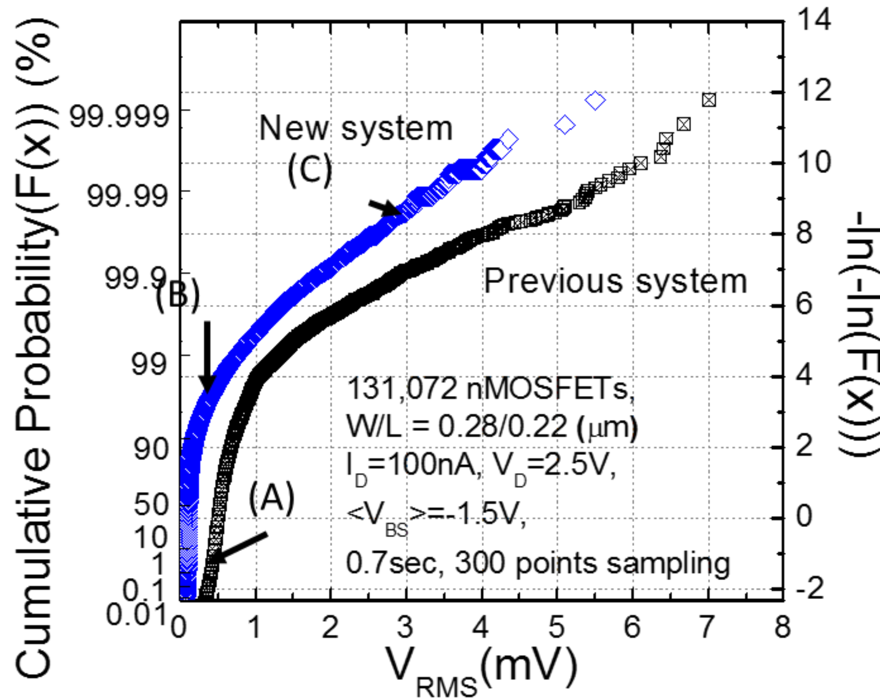


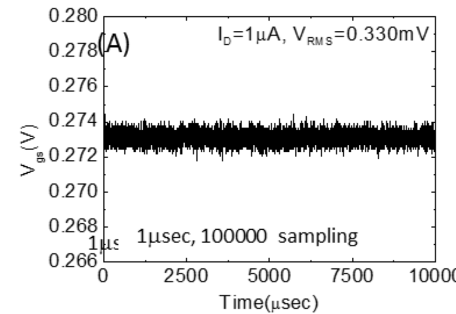
Y. Kumagai et al., Jpn. J. Appl. phys., 50, p. 106701, 2011.
K. Abe et al., VLSI. Technol. symp., p. 210, 2007.
S. Watabe et al., Jpn. J. Appl. phys., 46, p. 2054, 2007.
A. Yonezawa et al., IRPS, XT-11, 2013.

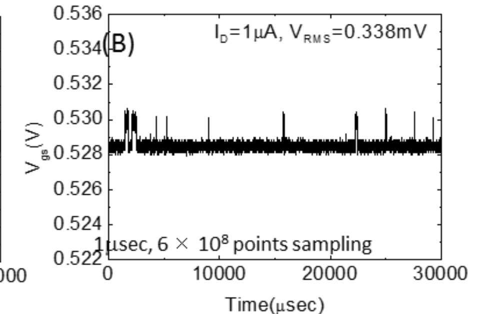
- On-Wafer Measurement System — Floor noise 400 μV
- On-Board Measurement System — Floor noise 67 μV

Effect of accurate measurement system

T. Obara, A. Yonezawa et al., SSDM, p.722, 2013.

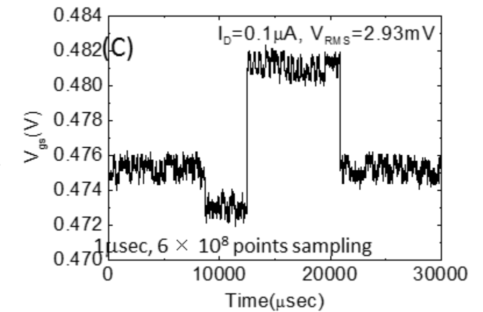






ノイズ強度:

$$V_{RMS} = \sqrt{\frac{\sum_{i=1}^{N}\left(V_{OUT,i} - \overline{V_{OUT}}\right)^2}{N-1}}$$

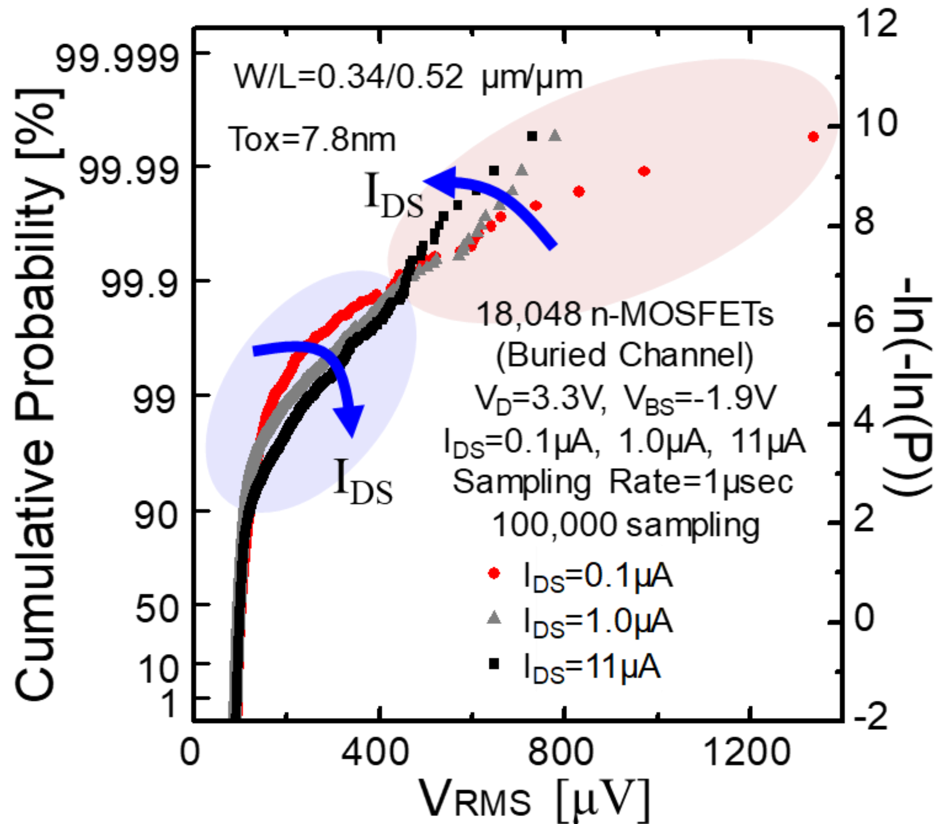


(B): We can observe the RTN wave form at the same V_{RMS} as former system.

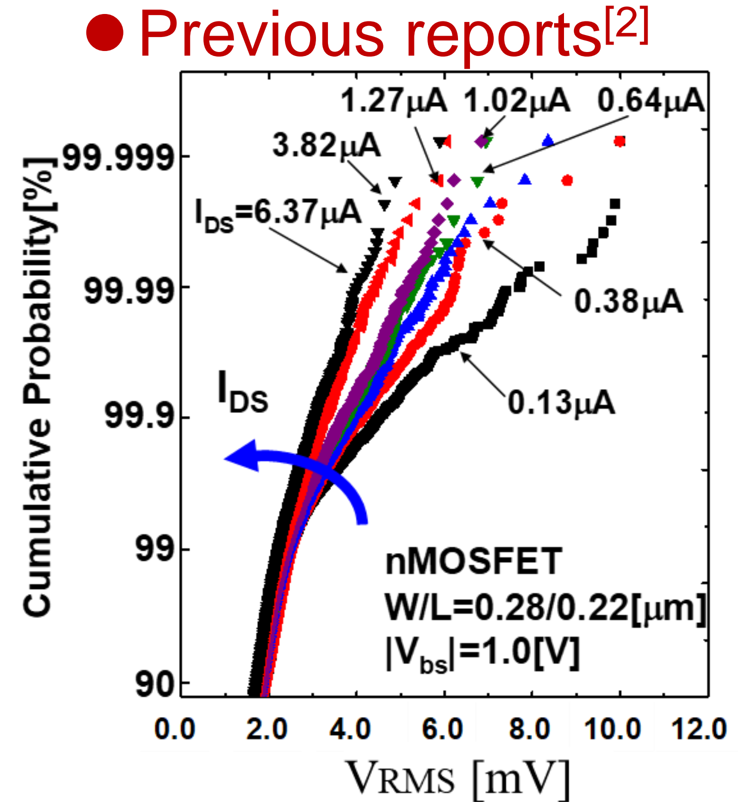
(C): Over 2 states RTN wave form can be observed,

⇒New system can observe the RTN wave form having low V_{RMS}.

Dependency of Drain Current to V_{RMS}



● Previous reports[2]



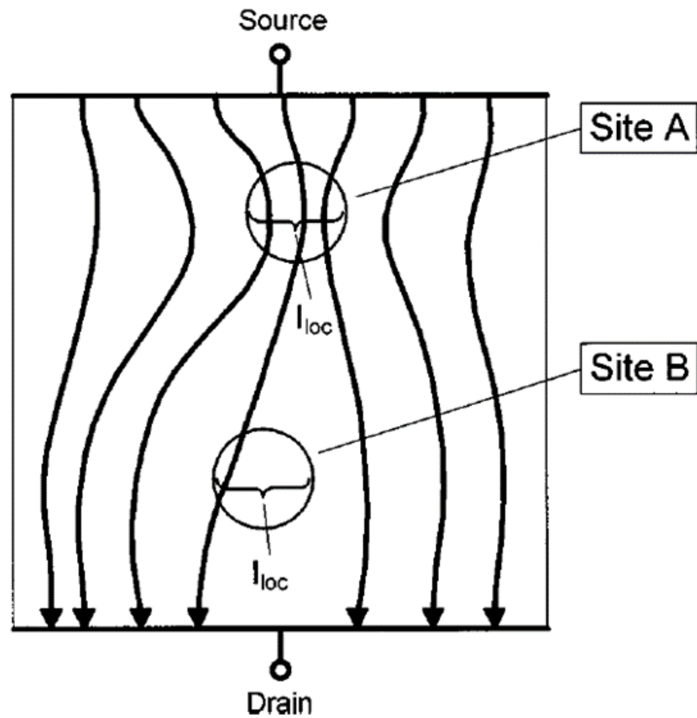
[2] *K. Abe, et al., Proc. Int. Image Sensor Workshop, p.62, 2007.*

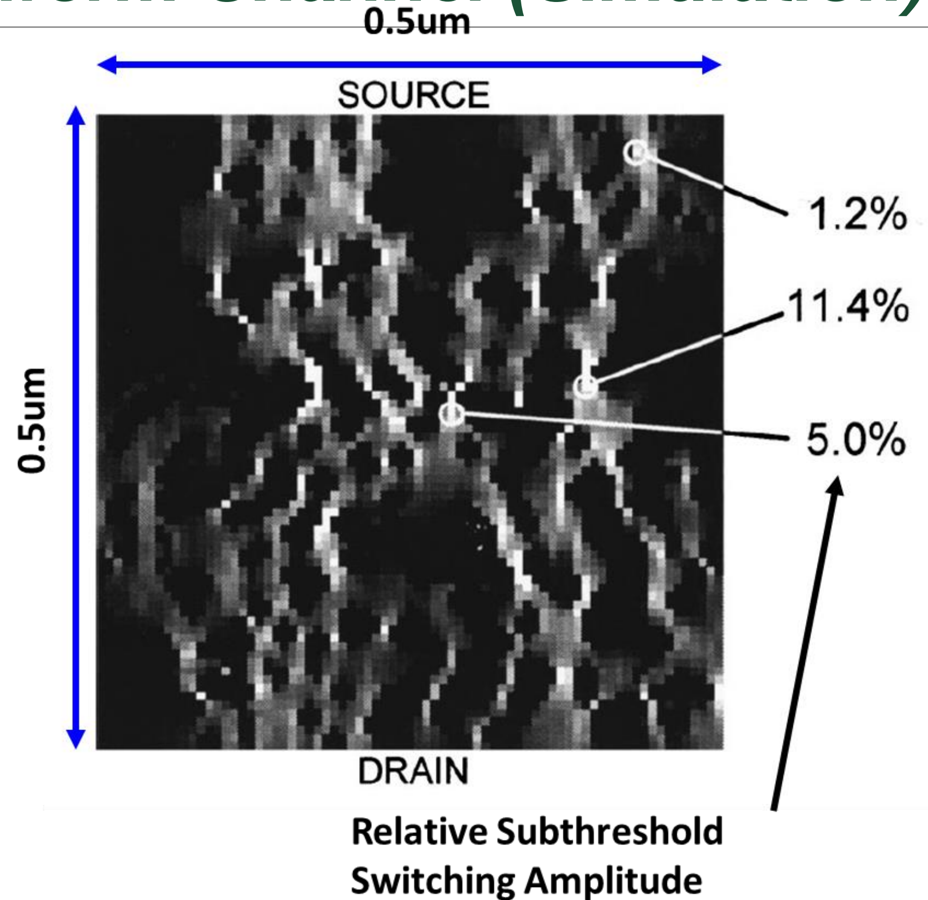
- VRMS in this graph is input referred value at floating diffusion node.
- Cumulative probability of about 99.9%-
  → VRMS becomes larger for smaller drain current.
- Cumulative probability of about 90% - 99.9%
  → VRMS becomes larger for larger drain current.

Previous reports*

New data

Amplitude of RTN in Non-Uniform Channel (Simulation)





RTS Amplitude: Site A > Site B

H. H. Mueller, et al., "Random telegraph signal: An atomic probe of the local current in field-effect transistors," J. Appl. Phys. Vol.83, pp.1734-1741, 1998

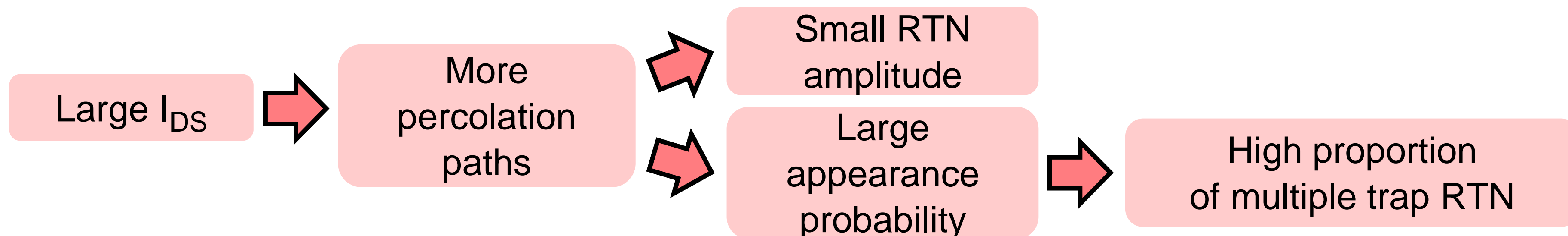
Impact of Drain Current to RTN

● I_{DS}=0.1μA
● I_{DS}=11μA

Case A
Drain
Source
RTN with large amplitude occurs.
Drain
Source
RTN with small amplitude occurs.
Empty trap

Case B
Drain
Source
RTN does not occur.
Drain
Source
RTN with small amplitude occurs.
Percolation path

Cumulative Probability
VRMS
11μA
0.1μA
Case A
Case B

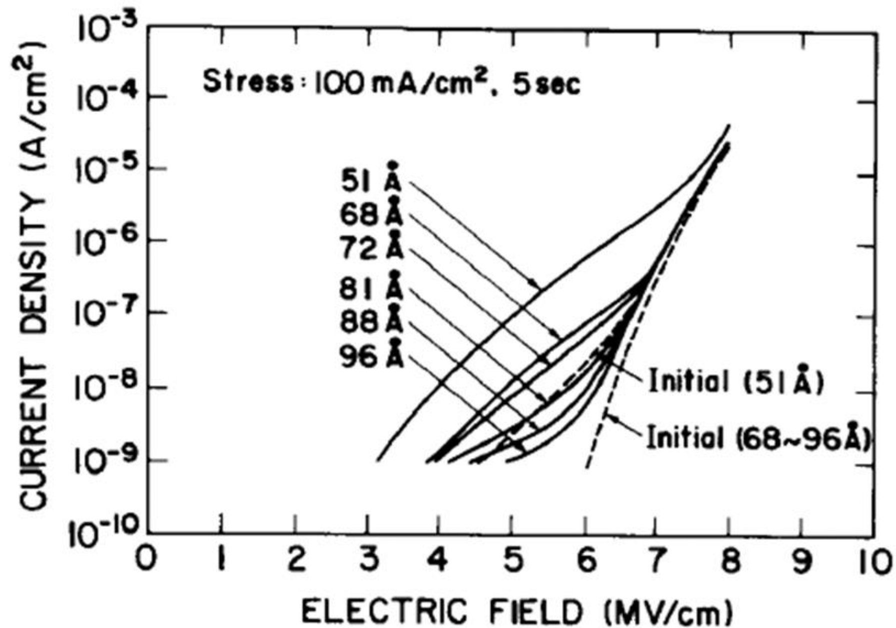


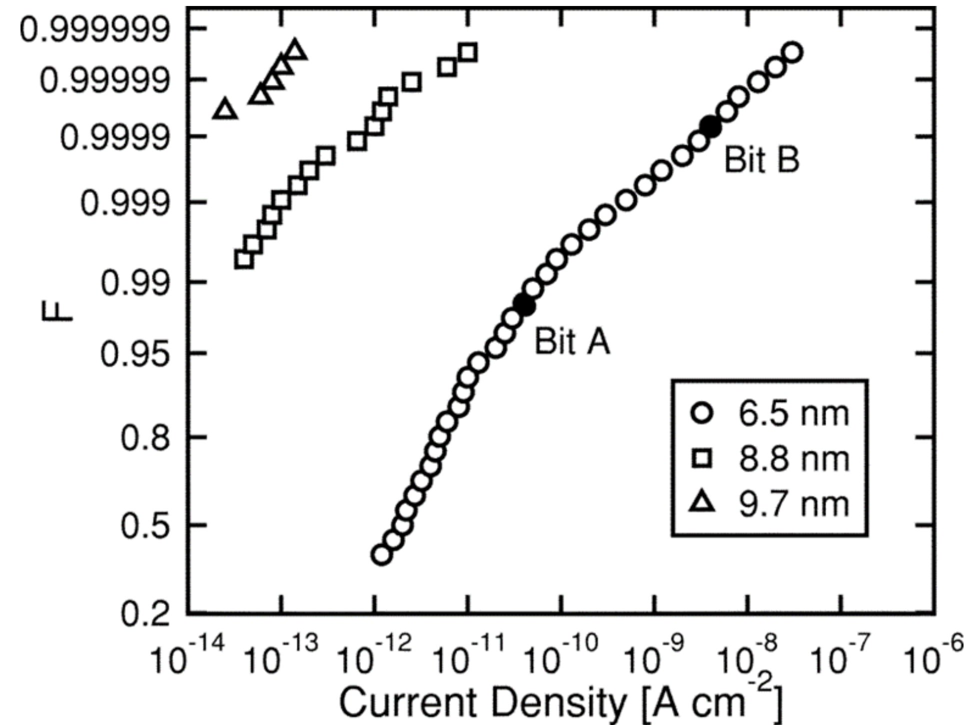
Case A : Impact of the traps to the percolation path increases.
Case B : Probability which traps influence percolation path increases.

絶縁膜のリーク電流

Stress Induced Leakage Current

SILC limits a shrinking tunnel oxide thickness

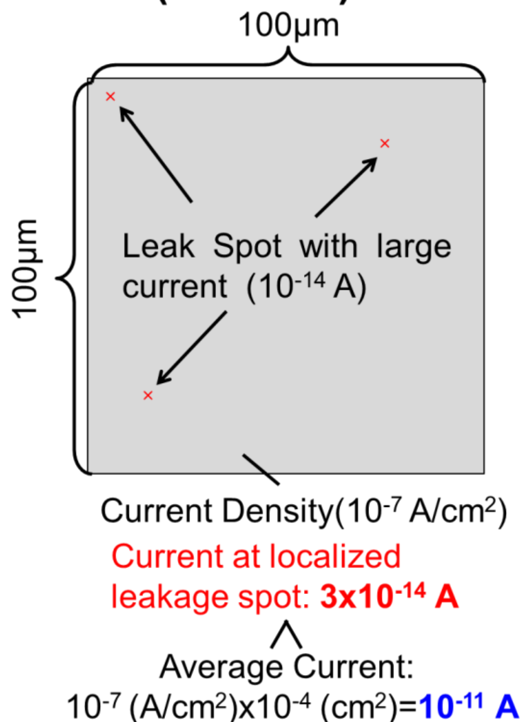


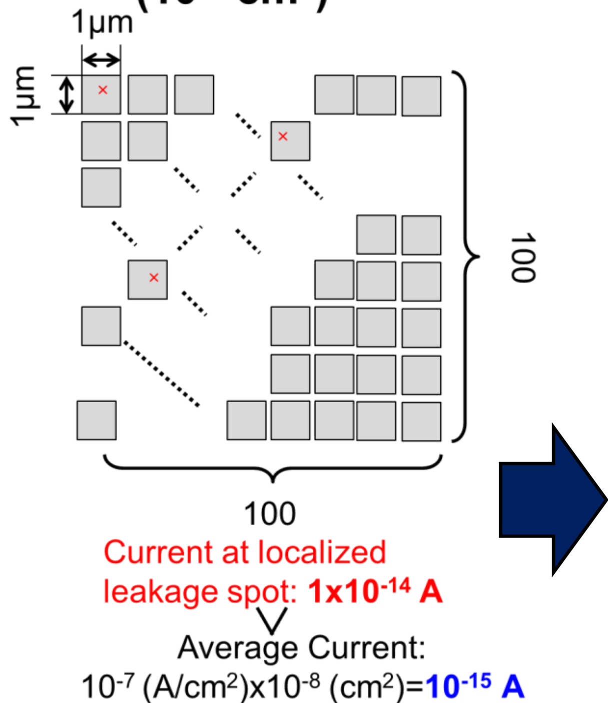


-Stress Induced leakage current (*SILC*) causes severe bit errors
-Tunnel oxide is thinner, SILC becomes larger.
- Localized leakage spot (trap) indicates large SILC

D. Ielmini, et al., Microelectron. Eng., 59, p.189 (2001).
R. Degraeve, et al., IEE Trans. Electron Devices, 51 p. 1392 (2004).

測定への要求





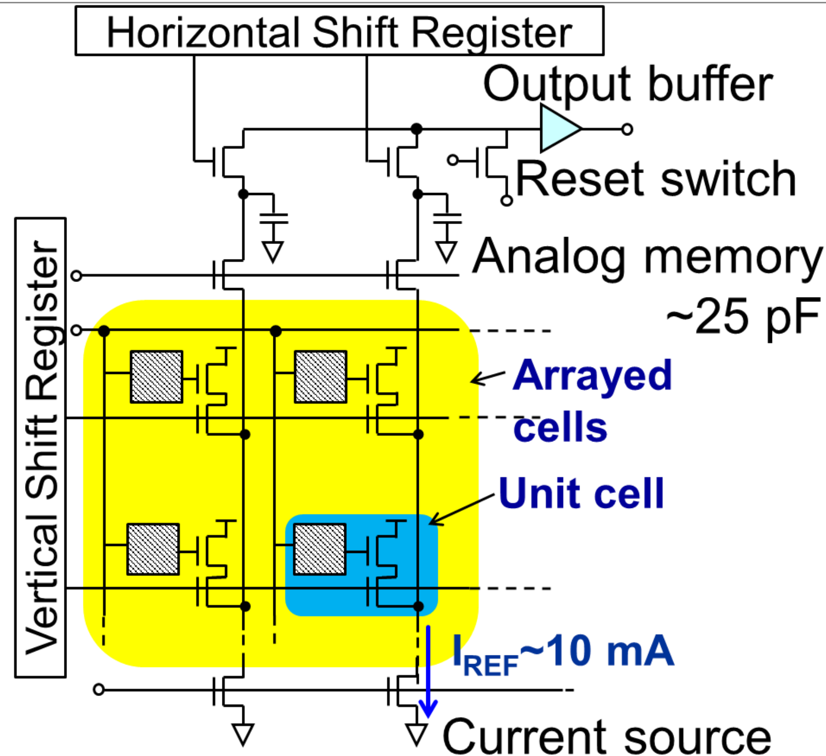
It is essentially required to measure

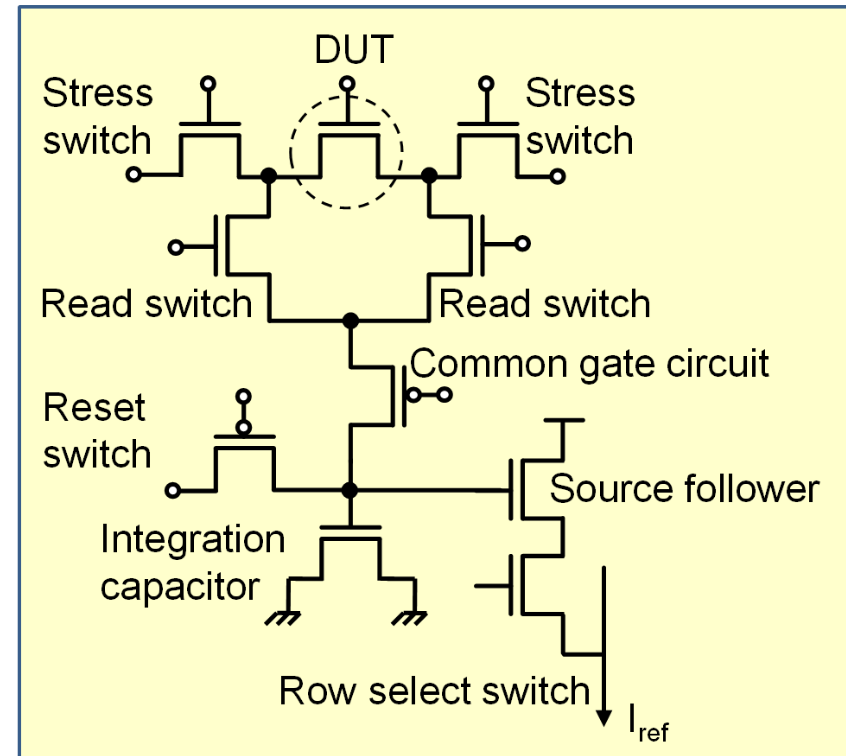
- **Sufficiently Small Size**
- **Sufficient number of MOSFETs**

However, Probability : 3/10000, Too small!!

Large leakage current (leakage spot)cannot be detected!

Test pattern for SILC measurement





Sufficient number of DUTs

Unit cells are arranged in matrix pattern→212^{V}x412^{H}=87344/shot

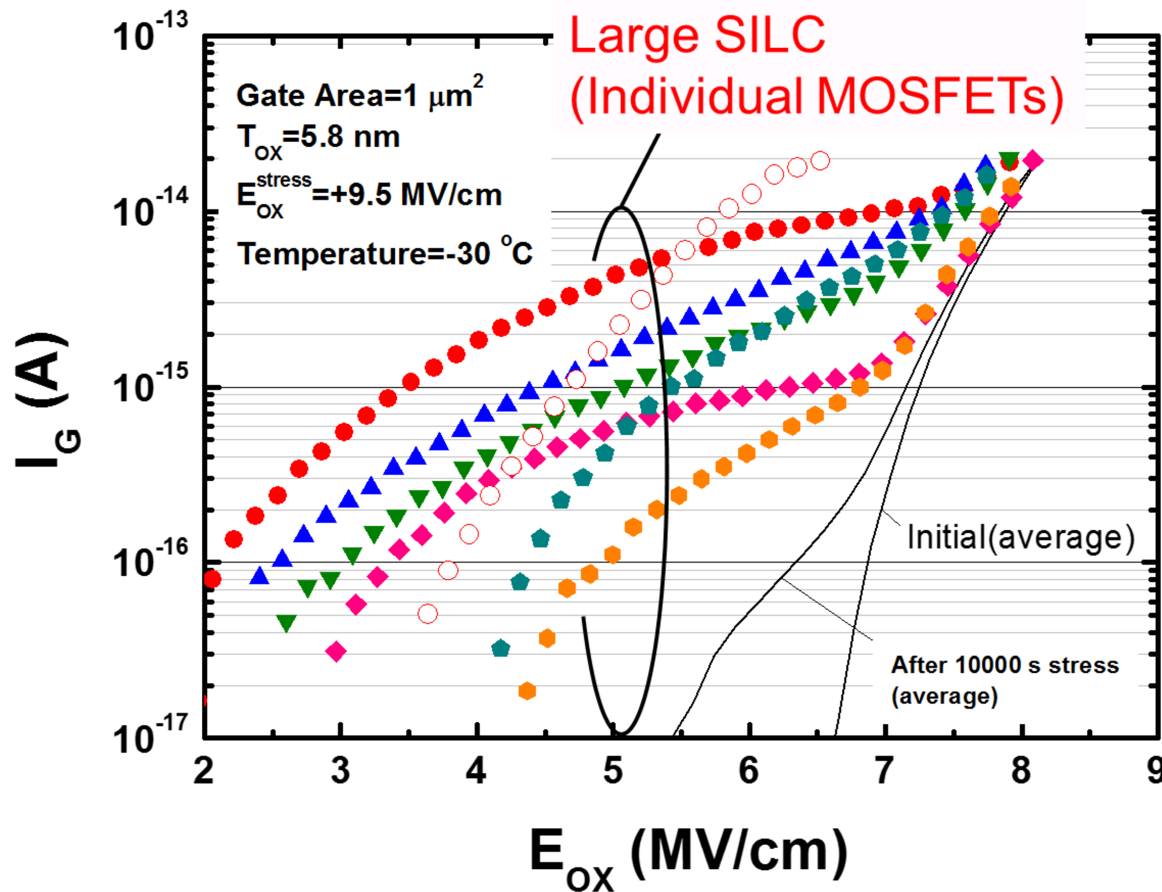
Short integration time and high accuracy

I_G is converted to voltage signal in unit cell by a capacitor (~14 fF)

High-speed sampling

87344 cells can be measured in 80 sec

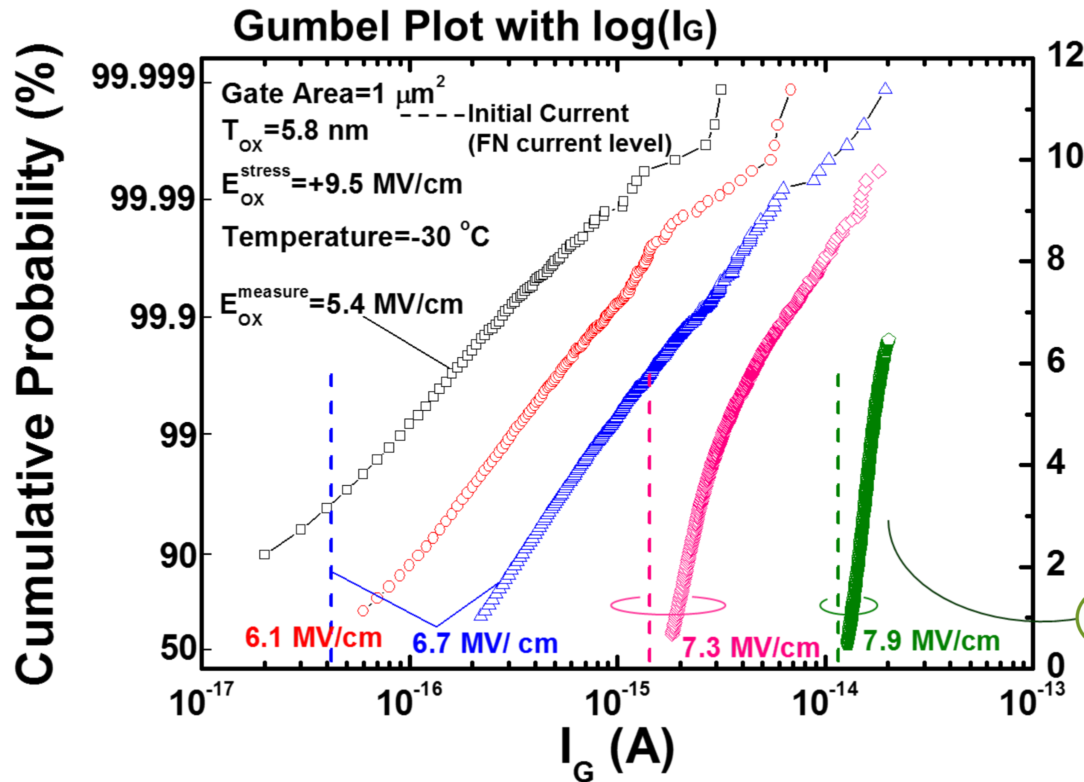
I_G-E_{OX} Characteristics of SILC

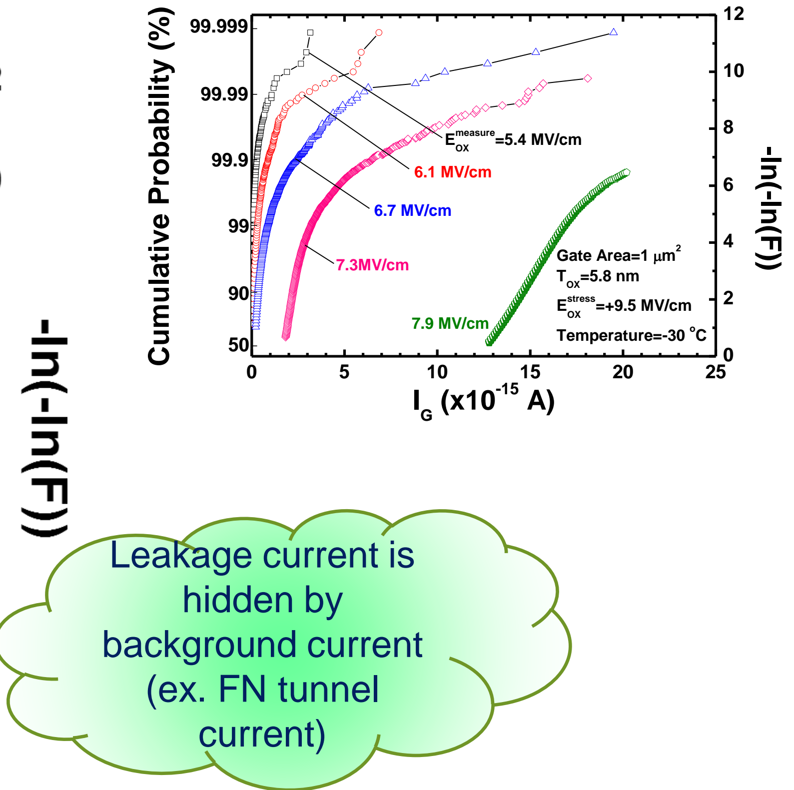


-By evaluation of very low current of 10^{-17} A, a large variety of leakage current can be observed.

-Even at 2 MV/cm, very large leakage current of 10^{-16} A flows the tunnel oxide.

Distribution of SILC





Distribution of log(I_G) (not linear I_G) at low E_{OX} region is on straight line on Gumbel plot. ***→The leakage current is defined by the current at a leakiest spot.***

まとめ

半導体デバイス

●Digital/Logicデバイス

デバイスサイズの微細化と高集積化が同時に進行
→デバイスサイズ:Sub-100nmからSub-10nmへ
集積度:100億-1000億Tr/chip

●Analog・高周波デバイス

Digitalデバイスほど微細化・集積化は進まず
←雑音、バラツキに対して敏感
＝デバイスの精度はDigitalデバイス以上のものが求められる。

評価技術:平均的特性、局所的特性を意識して評価することが重要